

**Compal Confidential**

**A740/A540 Schematics Document**

**INTEL Broadwell with DDR3L**

**AIO M/B**

**AUG. 1, 2013**

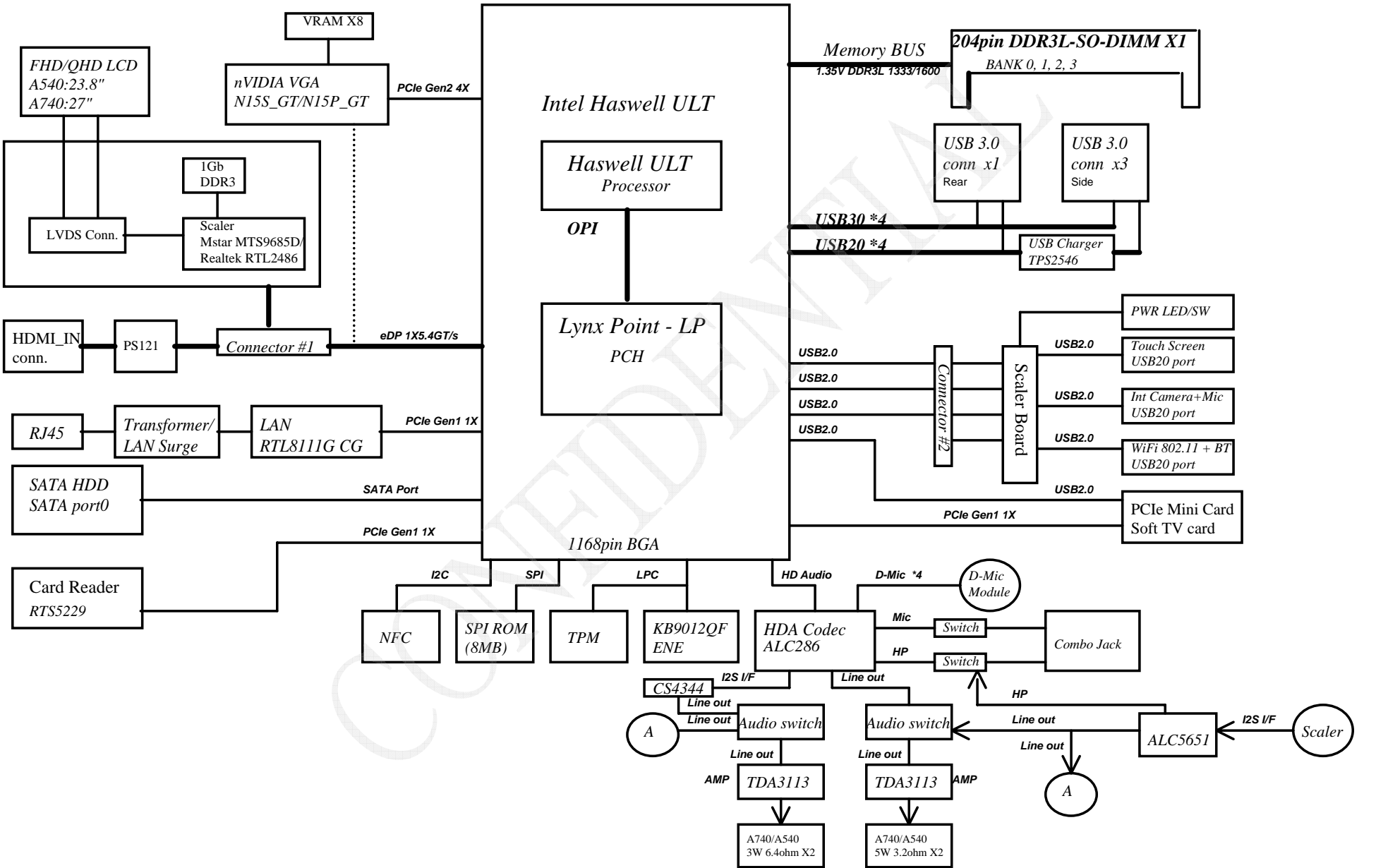
**REV: 0.1**

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Model Name : A740/A540

File Name :



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BOM Struecture Table

Function	Stuff	NC
UMA SKU	UMA@	
DGPU SKU	DIS@	
DGPU SKU (Power)	VGA@	@VGA@
DGPU support GC6	GC6@	
DGPU N14M-GL	N14M-GL@	
DGPU N14P-GV2	N14P-GV2@	
TPM	TPM@	
XDP	XDP@	
HDD re-driver	HDD_RD@	
HDD non re-driver	HDD@	
RTL8111G (LDO)	LAN_L@	
RTL8111GS (SW)	LAN_SW@	
PCH LPM support	PCH_LPM@	
ME Cnector	CONN@	
ESD Components	ESD@	@ESD@
EMI Components	EMI@ EMI@_VGA@ RF@_VGA@	@EMI@ @EMI@_VGA@ @RF@_VGA@
NC Components		@

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>BID</sub> min	V <sub>BID</sub> typ	V <sub>BID</sub> max	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D - 0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D - 0x30

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH	ON	ON	ON*
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTT power rail for CPU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF

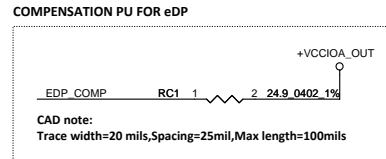
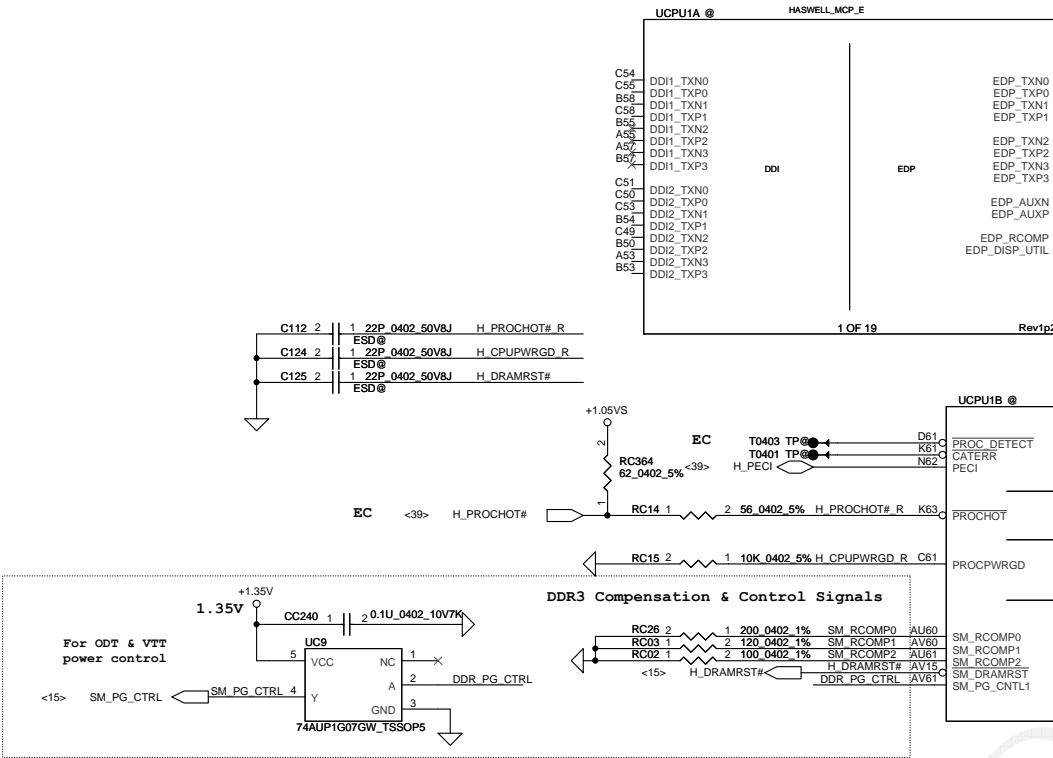
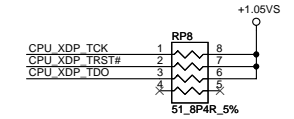


Table 5. Multiple Display Configuration for U-Processor Line

Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
HDMI	HDMI	eDP	4096x2304 @ 24 Hz	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz
DP	DP	eDP	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz
HDMI	DP	eDP	4096x2304 @ 24Hz	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz

Note: DP and eDP resolutions in this table are supported for 4 lanes with link data rate HBR2 at 24 bits per pixel (bpp) and single stream mode of operation.

#### CPU XDP Signals



## XDP CONN53.3.4 Processor Signals Connecting to XDP

Table 53-12. Processor Signals Connecting to extended Debug Port (XDP) Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
PREQ#		Point-to-point connection to OBSFN_A0 pin of XDP connector.	
PRDY#		Point-to-point connection to OBSFN_A1 pin of XDP connector.	
TCK0 TCK1	51Ω ±5% pull-down resistor on the trace and towards processor side of the trace	TCK0 should be routed directly between the XDP debug port and the processor TCK. TCK1—Leave TCK1 as a NO CONNECT. Provide exposed test-points for debug access for these pins.	
TMS		TMS should be routed directly between the XDP debug port and the processor. Provide exposed test-points for debug access for these pins.	
TRST#	51Ω ±5% pull-down resistor on the trace	This JTAG signal is routed as needed by the board design. It is suggested that TRST# be routed as a single daisy chain to all loads and terminated at the end of the trace. Provide exposed test-points for debug access for these pins.	
TDI		Point-to-point connection between the XDP connector and processor.	
TDO	Place a 51 Ω ±5% pull-up termination to VTAP near the PCH JTAG_TDI pin and place a pull-up 51 Ω ±5% termination resistor to VTAP on the TDO trace near XDR.	Point-to-point connection between the XDP connector and processor.	
DBR#	50-5 KΩ pull-up to 3.3VS	Connected to the HOOK7 pin of the Processor. Note: CRB uses a 1 KΩ pull-up to 3.3VS. On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.	

Table 53-12. Processor Signals Connecting to extended Debug Port (XDP) Checklist (Sheet 2 of 2)

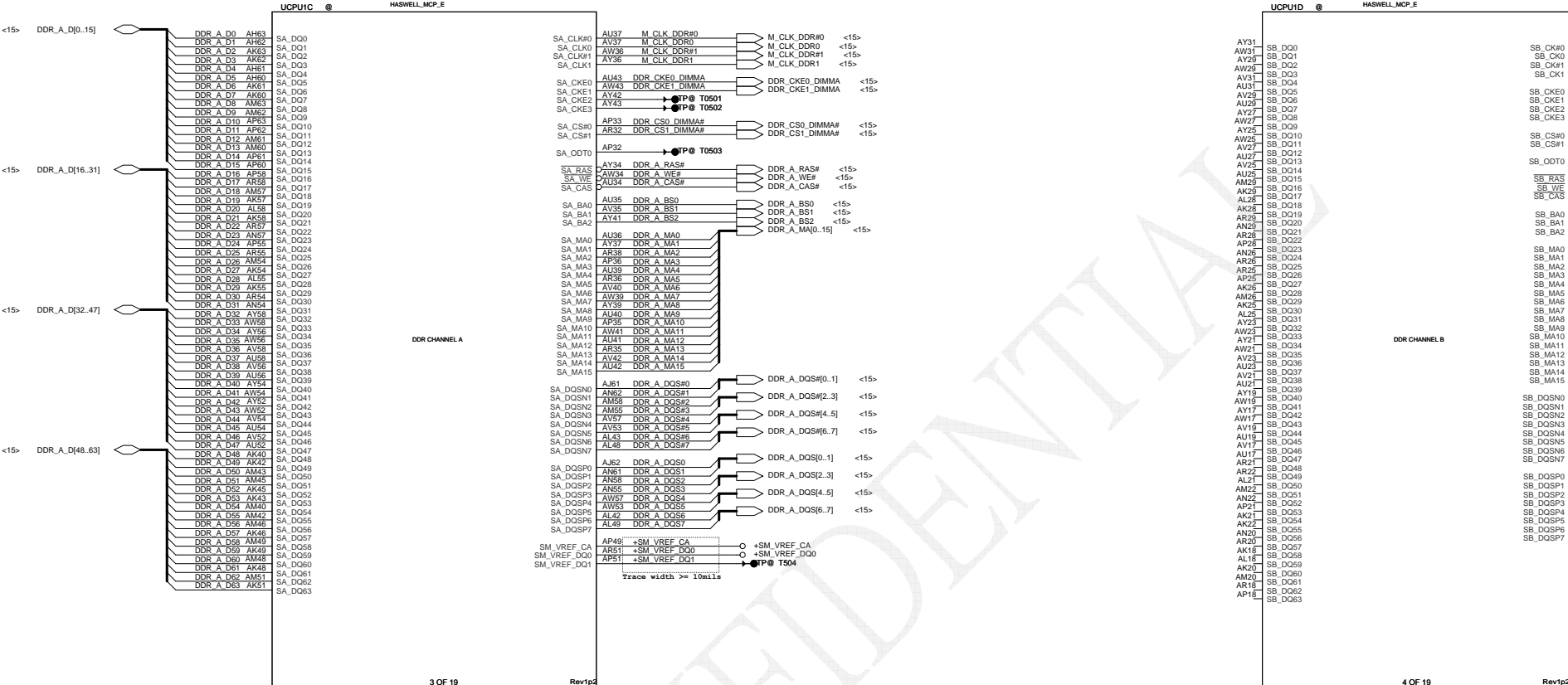
Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
BPM#[7:0]		Route the BPM#[7:0] signals point to point from the processor pin to the XDP debug (Not Implemented in 26 Pin Xdp Connector) port connector according to the Connectivity Table 53-13.	
PWR_DEBUG	150 Ω board level pull-up resistor to the PCH 1.05V VccCore on the trace	Connect to HOOK2 of Processor XDP connector. If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled.	
CFG[19:0]		Please refer to the Shark Bay and Denlow Platforms – Debug Port Design Guide	
CLKOUT_ITP_XDP_P/ CLKOUT_ITP_XDP_N		Route to Hook4 and Hook5 pins of XDP connector respectively. Refer to the latest Shark Bay and Denlow Platforms – Debug Port Design Guide.	
RSVD		These signals should be left NO CONNECT with open routing channels. These signals can be routed to test points.	

Note: The above signal list is for a 60-pin XDP connector. Refer to the latest version of the Shark Bay and Denlow Platforms – Debug Port Design Guide for more details on XDP connector for a complete list of 60-pin XDP signals and implementation details for 26-pin XDP connector.

Table 32. Testability Signals

Signal Name	Description	Direction / Buffer Type
BPM#[7:0]	<b>Breakpoint and Performance Monitor Signals:</b> Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O CMOS
PRDY#	<b>Processor Ready:</b> This signal is a processor output used by debug tools to determine processor debug readiness.	0 Asynchronous CMOS
PREQ#	<b>Processor Request:</b> This signal is used by debug tools to request debug operation of the processor.	1 Asynchronous CMOS
PROC_TCK	<b>Test Clock:</b> This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal must be driven low or allowed to float during power on Reset.	1 GTL
PROC_TDI	<b>Processor Test Data In:</b> This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	1 GTL
PROC_TDO	<b>Processor Test Data Out:</b> This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	0 Open Drain
PROC_TMS	<b>Processor Test Mode Select:</b> This is a JTAG specification supported signal used by debug tools.	1 GTL
PROC_TRST#	<b>Processor Test Reset:</b> This signal resets the Test Access Port (TAP) logic. This signal must be driven low during power on Reset. Refer to the appropriate processor Debug Port Design Guide (see Related Documents section) for complete implementation details.	1 GTL

Interleaved Memory



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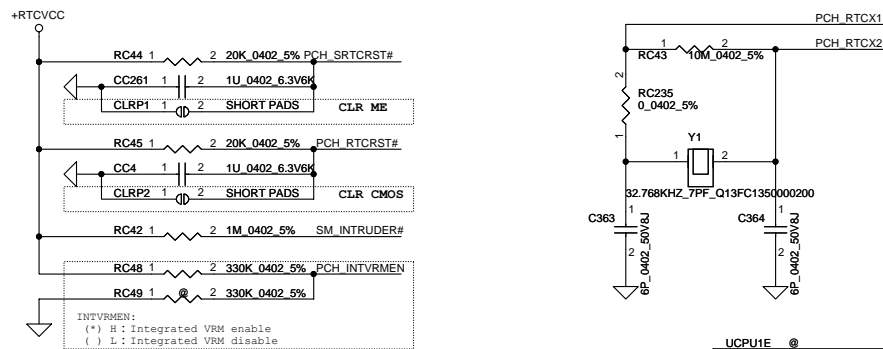
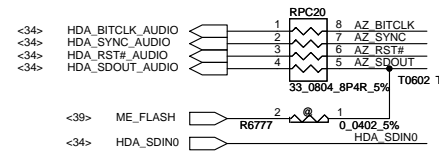


Figure 21-1. High Speed I/O (HSIO) Port Options

HSIO Port	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB3.0	1	2	3	4										
PCIe			1	2	3	4	5-L0	5-L1	5-L2	5-L3	6-L0	6-L1	6-L2	6-L3
SATA											3	2	1	0
GbE	soft strap values ->				000	001	010	011	100	101				

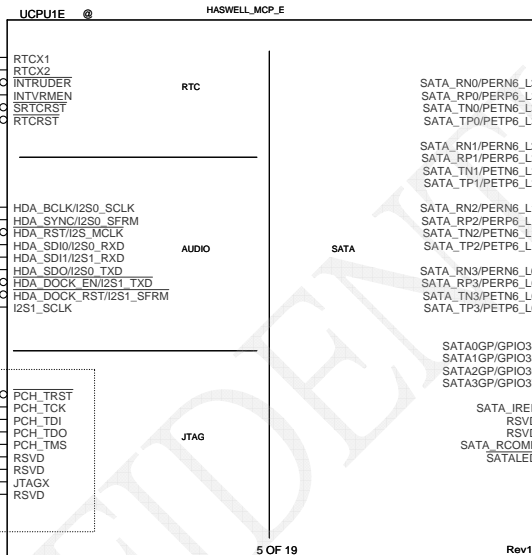
### HDA for AUDIO



### PCH JTAG

Connect to XDP Conn.  
(Option w/ CPU JTAG)

PCH_JTAG_RST#	AU62
PCH_JTAG_TCK	AE62
PCH_JTAG_TDI	AD61
PCH_JTAG_TDO	AE61
PCH_JTAG_TMS	AD62
AL11	
AC4	
AE63	
AV2	



For selected technology (PCIe or SATA),  
please use 100nF AC coupling

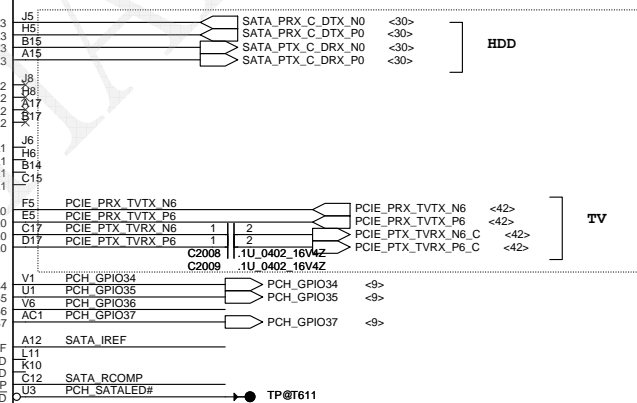
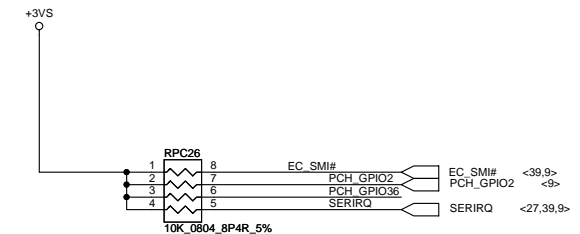
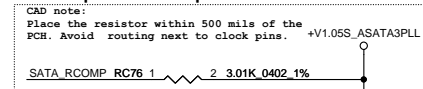


Table 53-14. PCH Signals Connecting to XDP Checklist

Pin Name	System Pull-up/Pull-down	Schematic Notes	
TCK0	A pull-down 51Ω, ±5% termination resistor should be placed at the end of the trace.	TCK0 should be routed to PCH JTAG_TCK pin.	✓
TDI TDO	Place a 51Ω, ±5% pull-up termination to VTAP near the PCH JTAG_TDI pin and place a pull-up 51Ω, ±5% termination resistor to VTAP on the TDO trace near XDP.	Route the TDI and TDO from the debug port to the PCH JTAG_TDI and JTAG_TDO	
TMS	Place a pull-up 51Ω, ±5% termination resistor to the VTAP at the end of the trace.	Routed to PCH JTAG_TMS pin	
TRST#		This JTAG signal is not included in the PCH pin map. The PCH signal TRST# is not a TAP TRSTn pin. Leave the XDP TRSTn pin unconnected for this debug port. Consult the Platform Design Guide (PDG) for routing guidelines of PCH TRST# pin.	

**Note:** The above signal list is for a 60-pin XDP connector. Refer to the latest version of the *Shark Bay and Denlow Platforms - Debug Port Design Guide* for more details on the XDP connector and for a complete list of 60-pin XDP signals and implementation details for the 26-pin XDP connector

### SATA Impedance Compensation



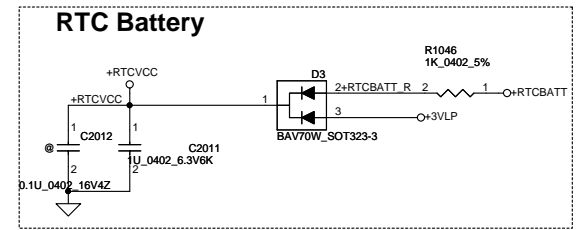
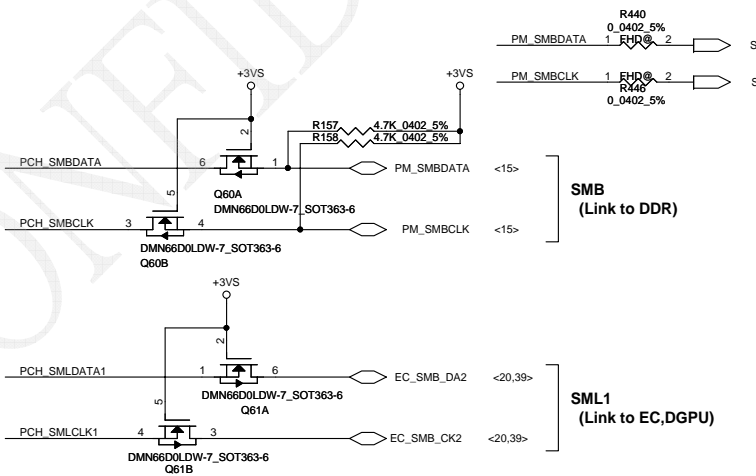
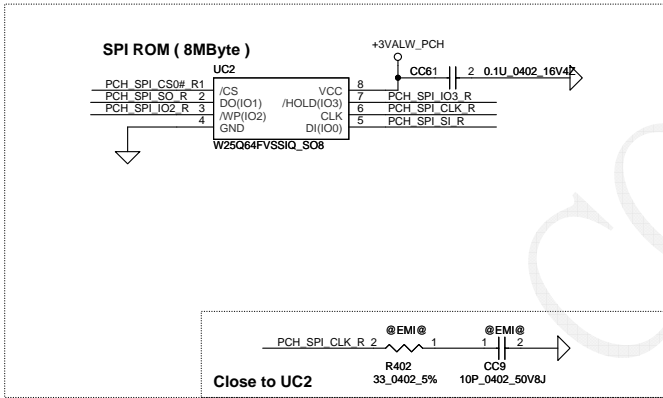
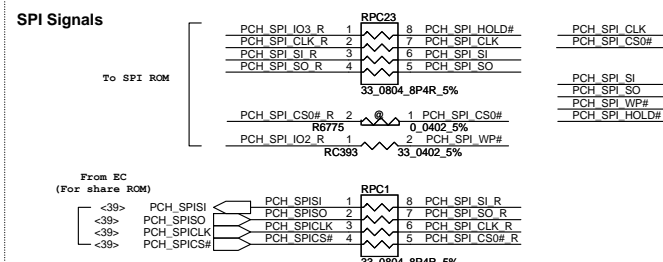
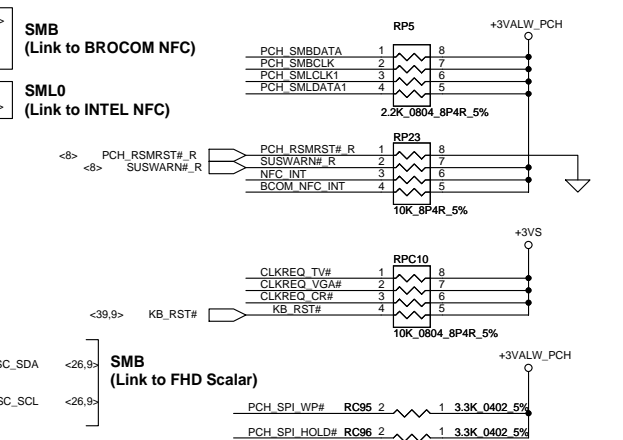
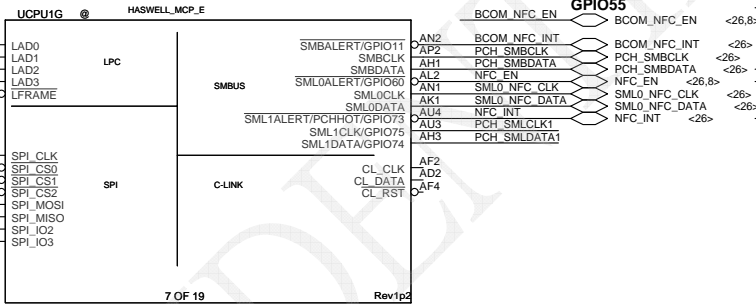
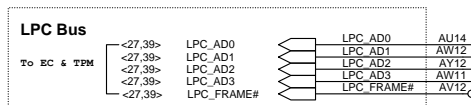
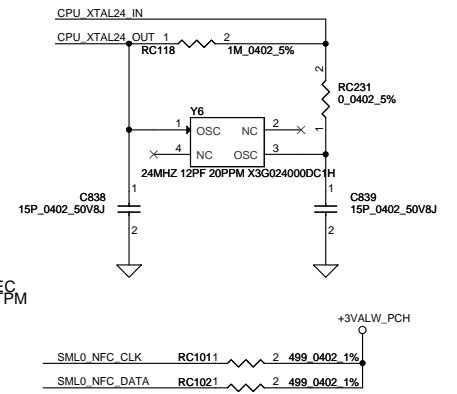
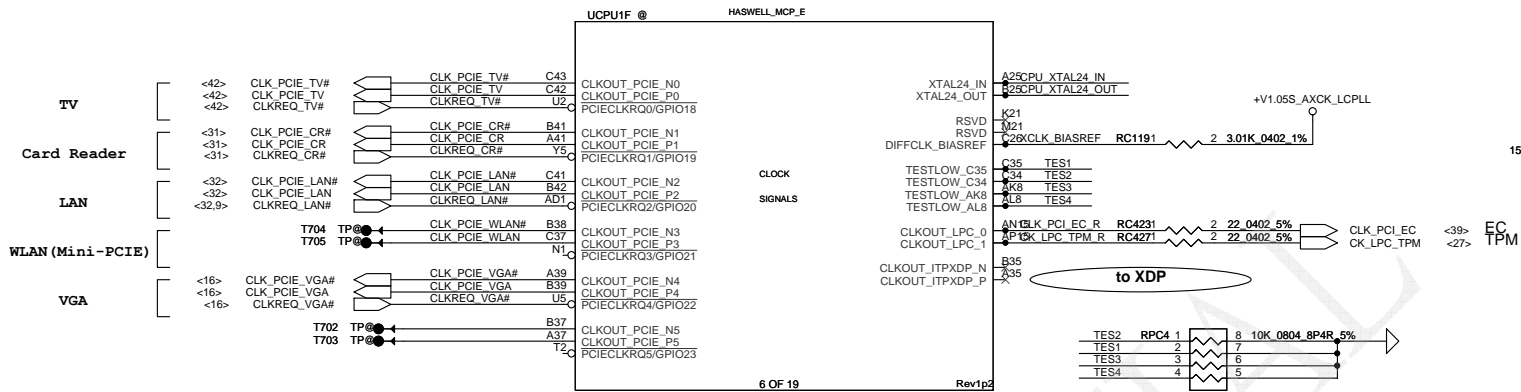
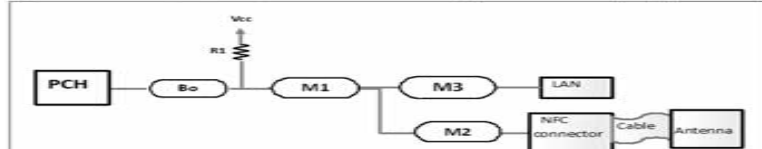
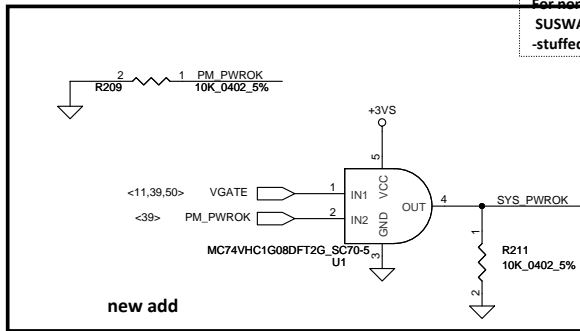


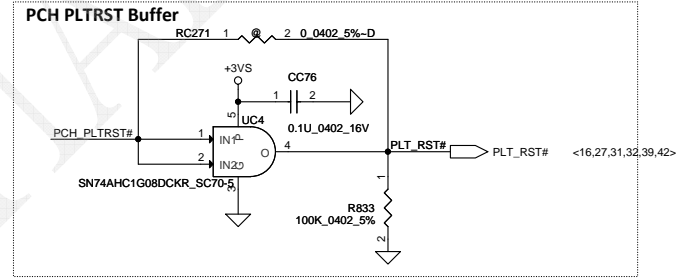
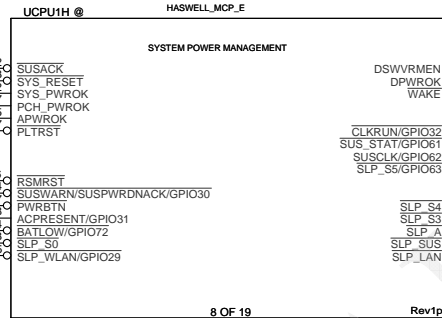
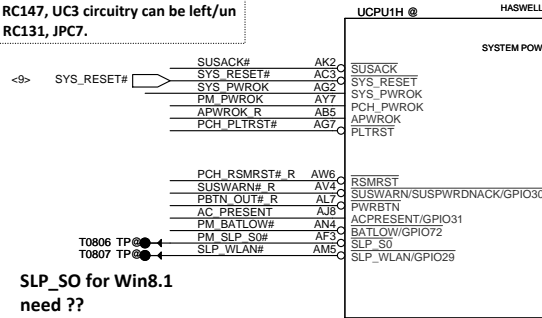
Figure 46-3. PCH SMLink0 to NFC Connector Layout Branch Topology



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For non-DSW supports, SUSACK(AK2), SLP\_SUS(AP4), SUSWARN(AV4), RC147, UC3 circuitry can be left/un-stuffed and stuff RC131, JPC7.



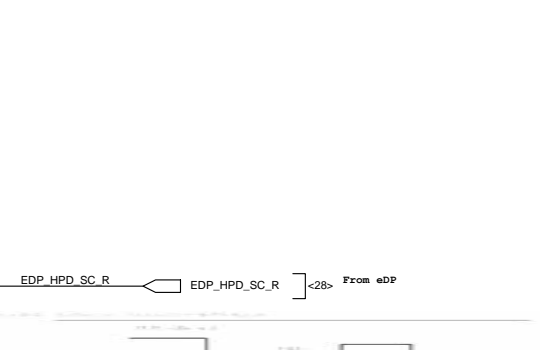
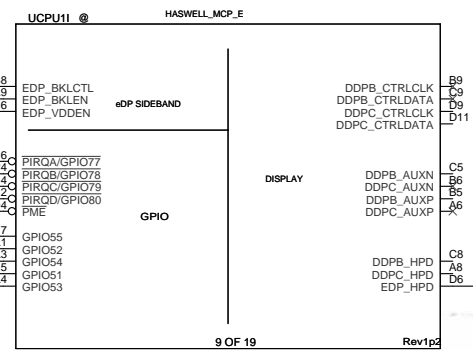
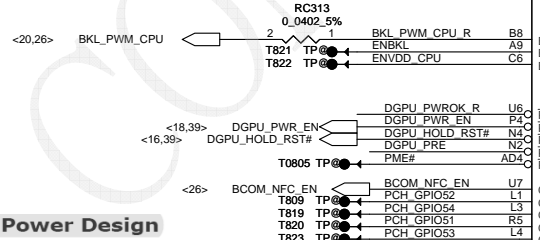
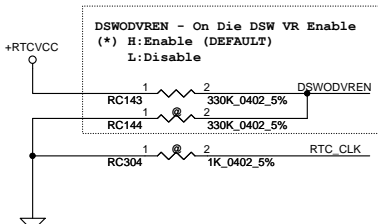
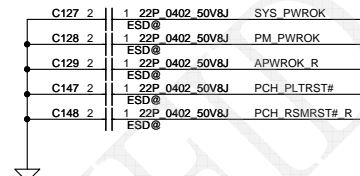
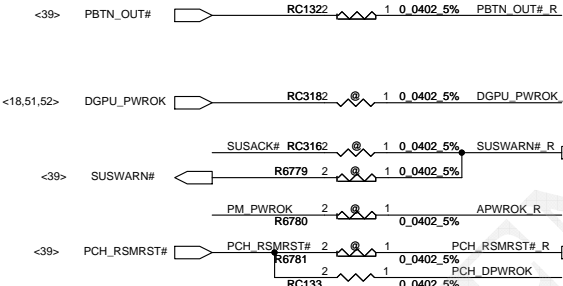
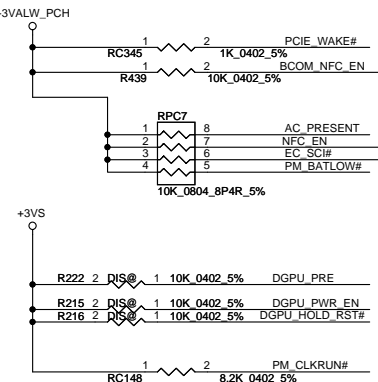
On systems that support Deep Sx the SLP\_WLAN# signal is used as an indication from Intel® ME as to whether the WLAN device should be powered or not.

The WLAN should be powered if:

- SLP\_A# = 1 (Intel® ME is in M0 or M3 and needs power)
- SLP\_WLAN# = 1 (Intel® ME may need wireless wake capability)

When the Intel® ME enters M-Off and needs the WLAN to stay powered, it de-asserts the SLP\_WLAN# pin. If the Intel® ME enters M-Off with no need for the WLAN to stay powered, it asserts the SLP\_WLAN# pin.

The WLAN power must be stable before the Intel® ME asserts the APWROK signal.



### 53.8.3 Windows\* 8.1—Connected Standby Low Power Design Recommendations

Table 53-59. Connected Standby Low Power Design Recommendations (Sheet 1 of 4)

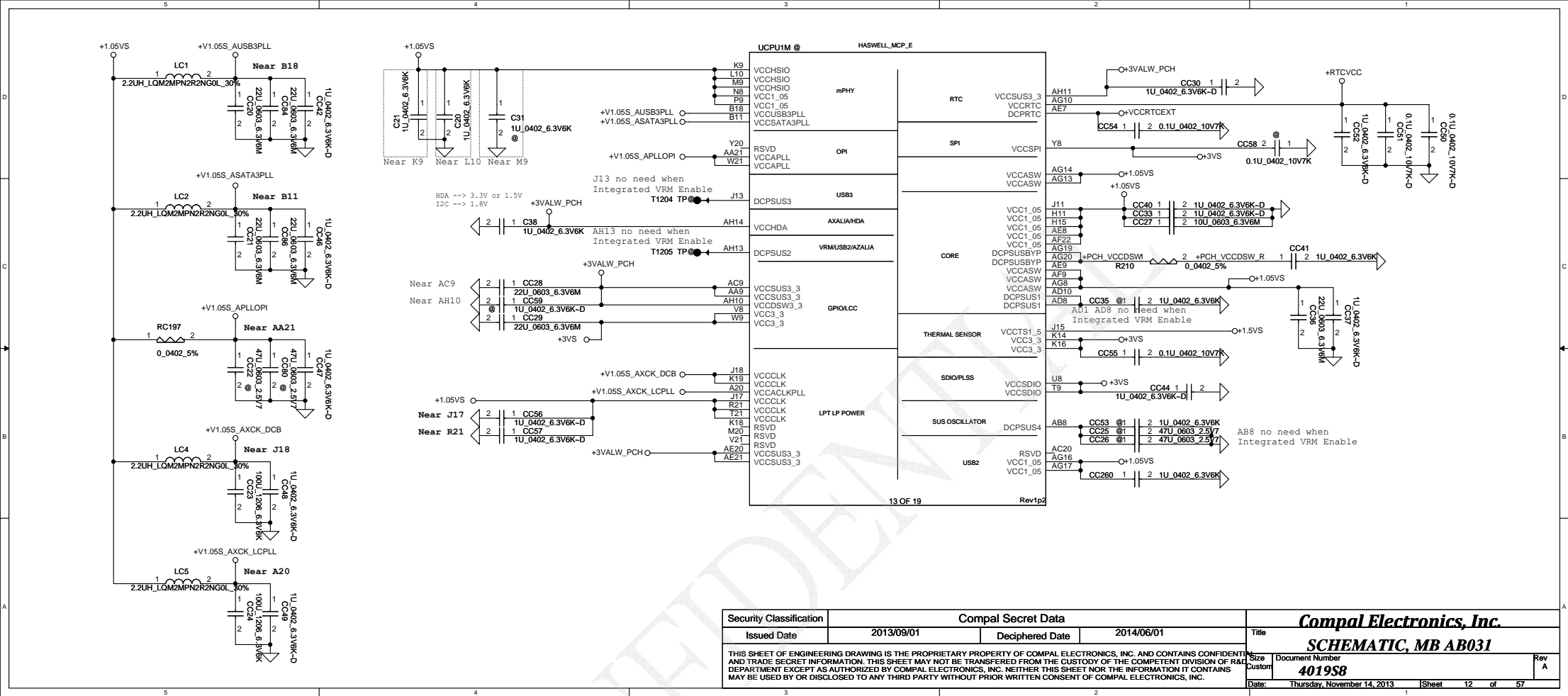
Component	Signal Name	Notes
Voltage Regulators	SLP_S0#	<ul style="list-style-type: none"> <li>• SLP_S0# should not be used as an indicator of Connected Standby to power gate discrete logic</li> <li>• SLP_S0# should be routed to EC and platform VRs as applicable. OEMs should select VR controllers that support SLP_S0# functionality if this signal is routed to the system VRs. Refer to the Shark Bay Ultrabook™ Platform Power Architecture Design Guide for SLP_S0# usage details.</li> <li>• For more details see Crescent River Power Management Integrated Circuit (PMIC) Specification, section on low power mode indicator SLP_S0#.</li> </ul>

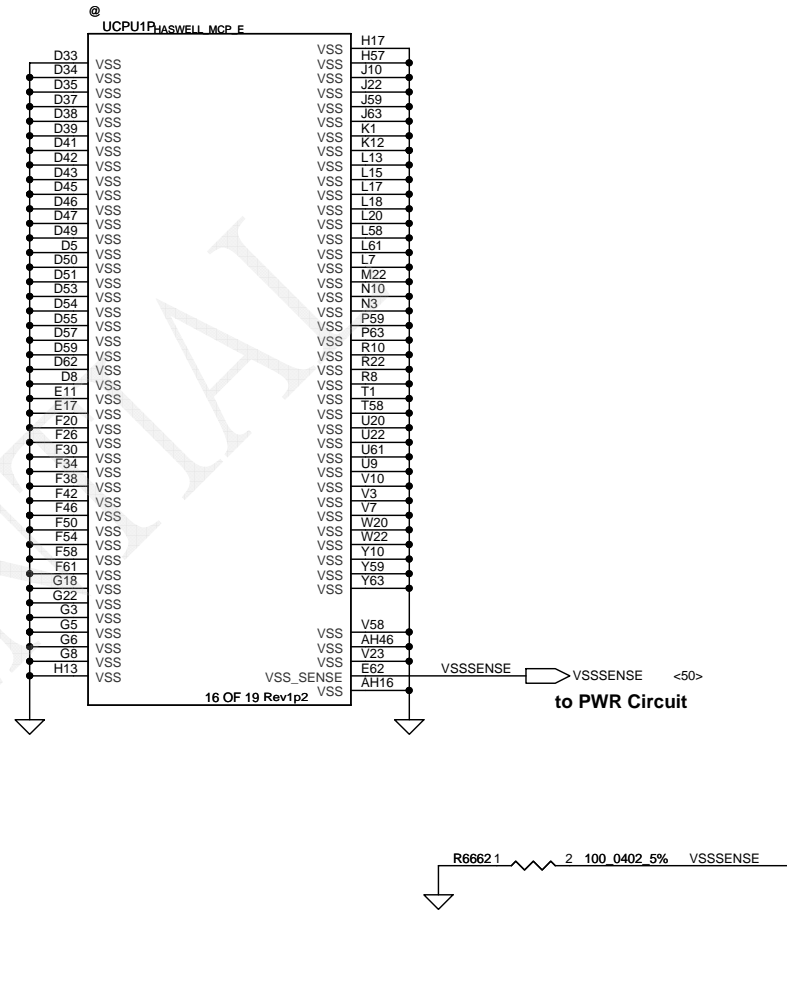
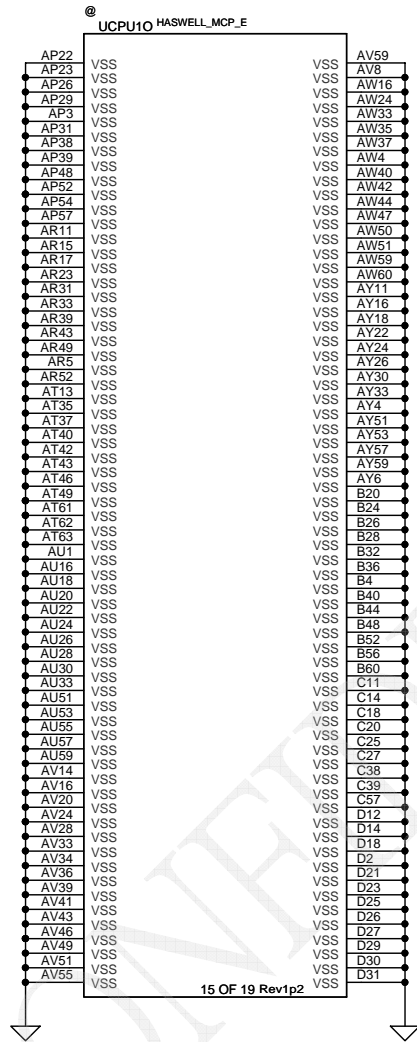
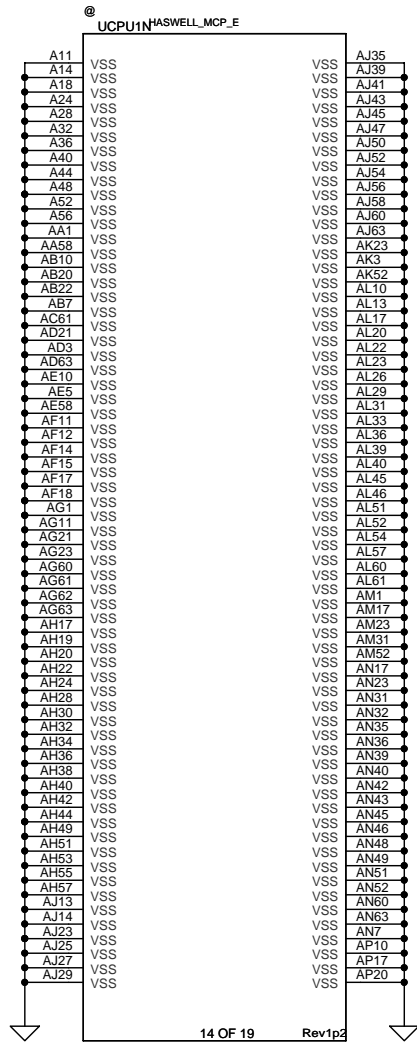




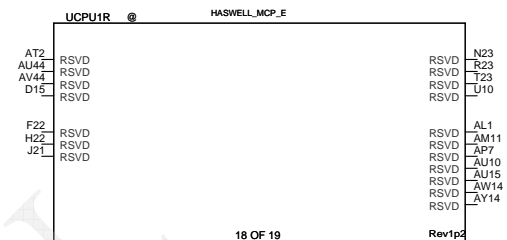
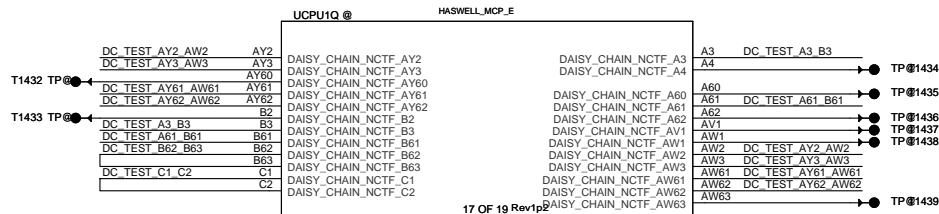




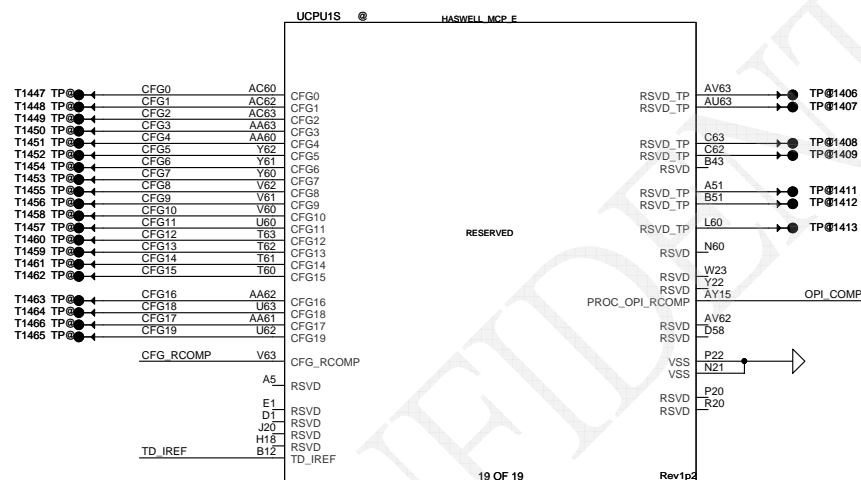
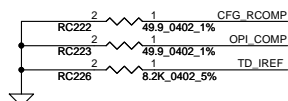




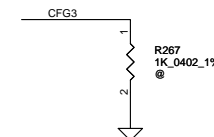
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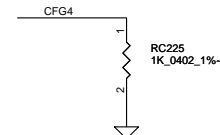
# CFG Signals (For Strap & XDP)



## CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port







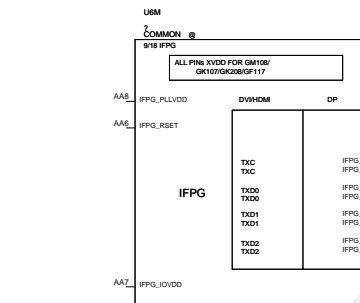
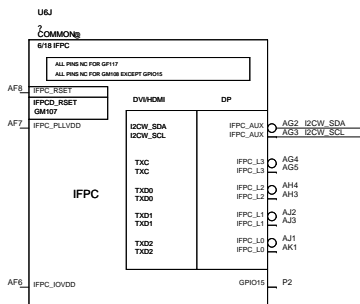
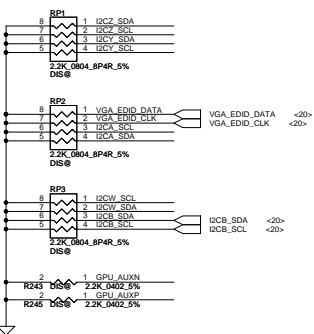
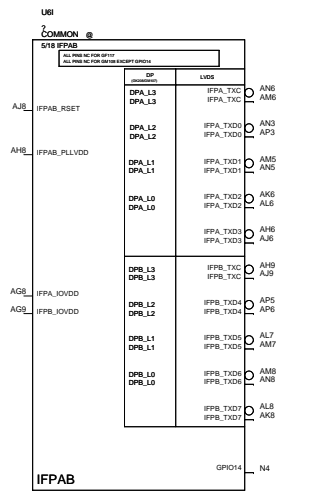
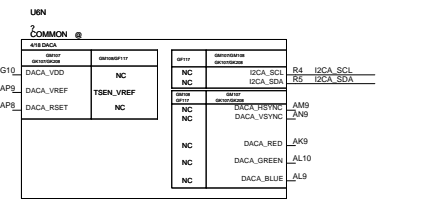
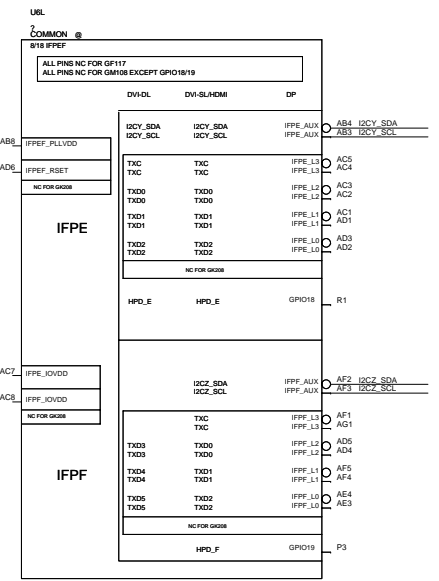
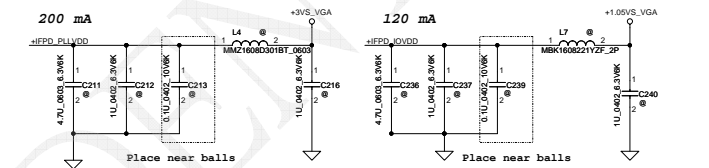
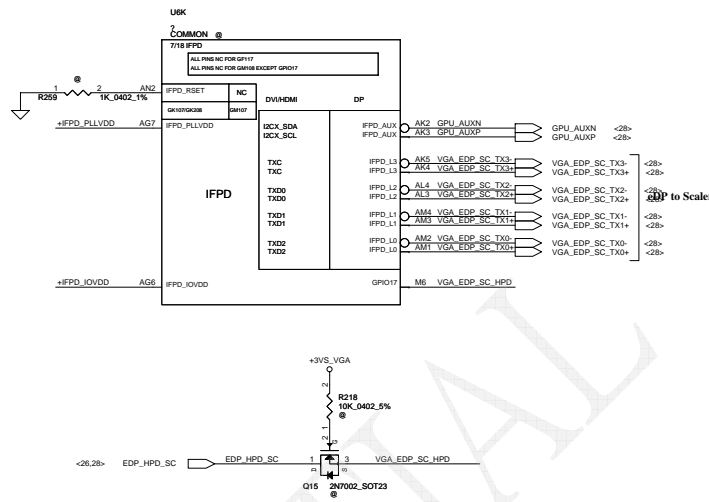
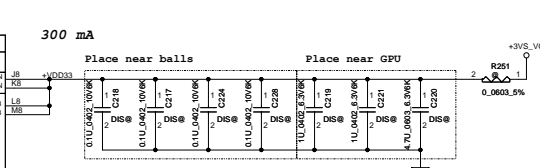
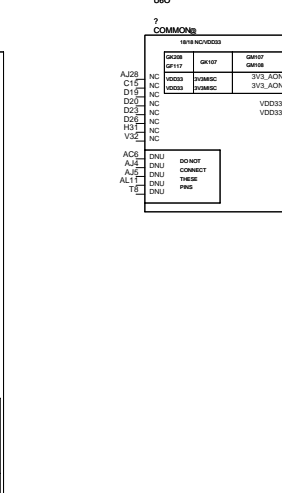
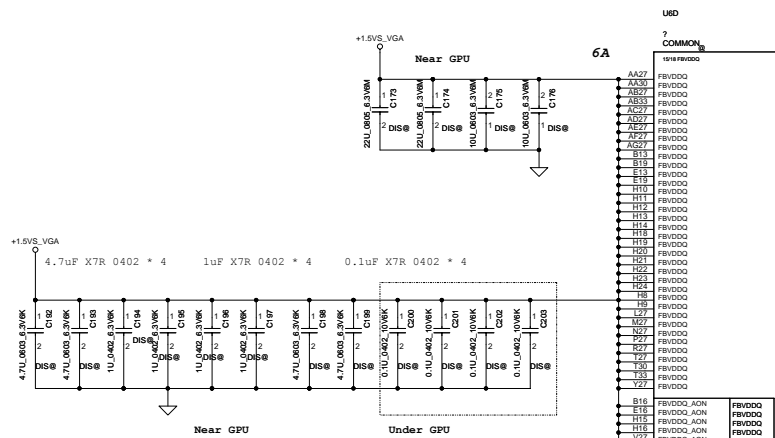


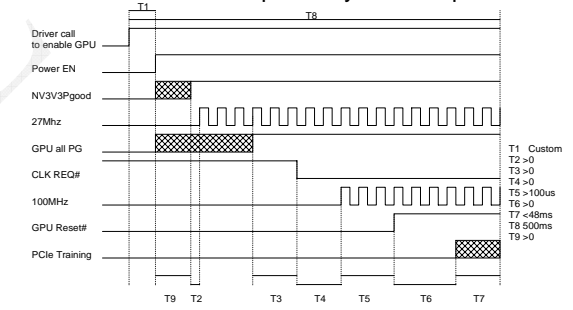
Table 8-1. H15x Family Display Link Summary

Link	Description
GB4B-128 Standard Mode	
Link A	LVDS (Dual Link) / DVI (Single or Dual Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link with IFPF)
Link F	DisplayPort (When Link E is not used), DVI (Dual Link with IFPF)
GB4B-128 Split Mode AB	
Link A	DisplayPort, DVI (Single Link)
Link B	DisplayPort, DVI (Single Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link EF	Not Connected
GB4B-128 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link)
Link F	DisplayPort/eDP, DVI (Single Link)

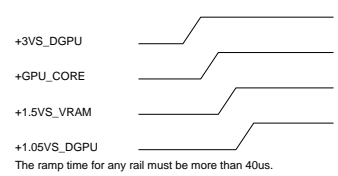




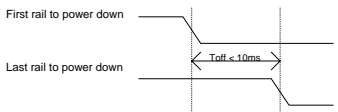
GPU Power Up Sub-system Sequence



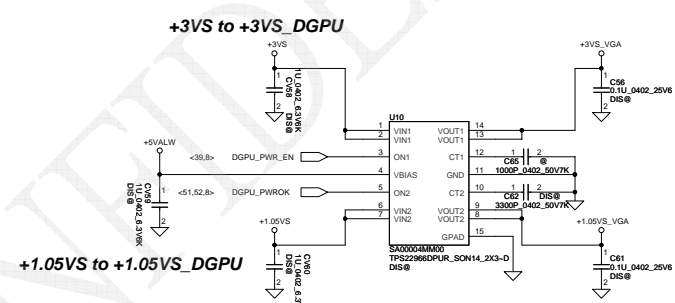
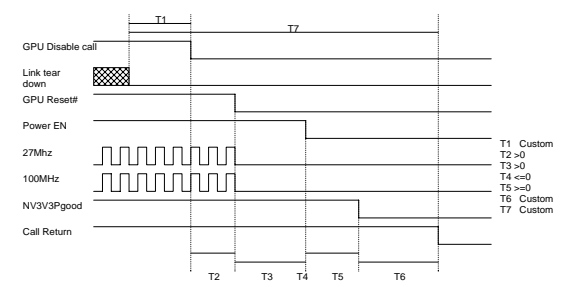
GPU Power Up Power Rail Sequence



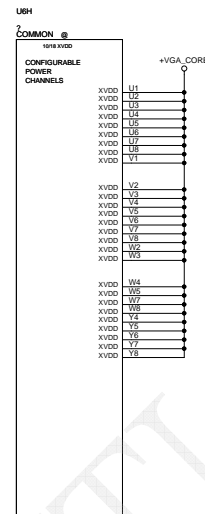
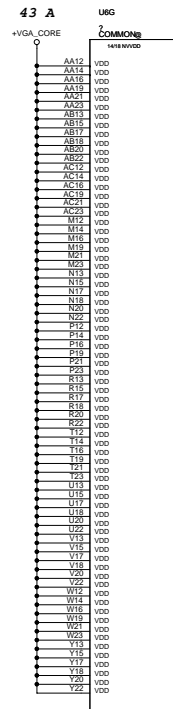
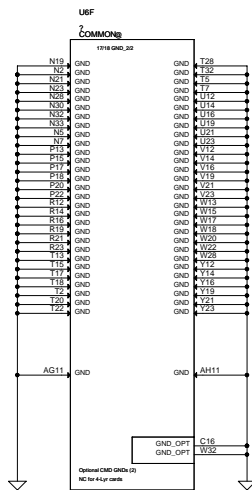
GPU Power Down Sequence



GPU Power Down Sub-system Sequence



CALIBRATION PIN	DDR3
FB CAL x PD VDDQ	40.2Ohm
FB CAL x PU GND	42.2Ohm
FB CAL xTERM GND	51.1Ohm



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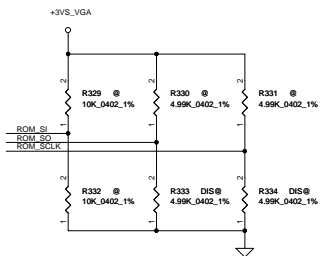


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep pull-up to VDD_AON and pull-down to GND foot print and stuff 50kΩ pull-up			
STRAP1	RESERVED			
STRAP2				
STRAP3				
STRAP4				

## 10.2 I<sup>2</sup>C AVAILABILITY

Table 10-2. I<sup>2</sup>C Availability

Bus ID	Signal Name	Type	Application	Associated Display Link	Voltage Tolerance
A	I2CA_SDA, I2CA_SCL	Bus master	DDC	DAC A - CRT	5 V
B	I2CB_SDA, I2CB_SCL		DDC and external devices	IFPA, IFPB - LVDS	
C	I2CC_SDA, I2CC_SCL		External devices	N/A	
S	I2CS_SDA, I2CS_SCL		Internal thermal sensor	N/A	
W	IFPC_AUX, I2CW_SDA, N IFPC_AUX, I2CW_SCL	Bus master	AUX/DDC	IFPC	3.3 V
X	IFPD_AUX, I2CX_SDA, N IFPD_AUX, I2CX_SCL		AUX/DDC	IFPD	
Y	IFPE_AUX, I2CY_SDA, N IFPE_AUX, I2CY_SCL		AUX/DDC	IFPE, IFPA-DP	
Z	IFPF_AUX, I2CZ_SDA, N IFPF_AUX, I2CZ_SCL		AUX/DDC	IFPF, IFPB-DP	

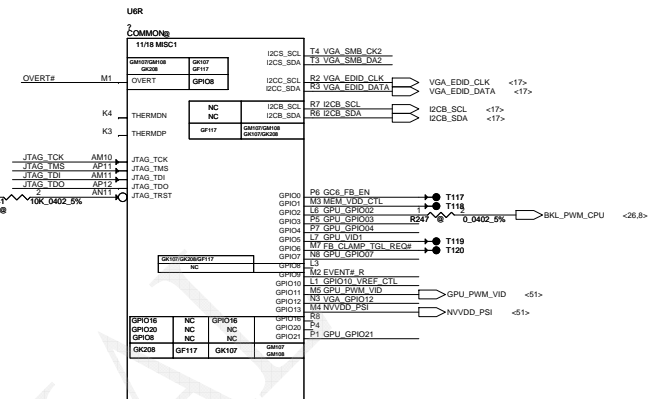
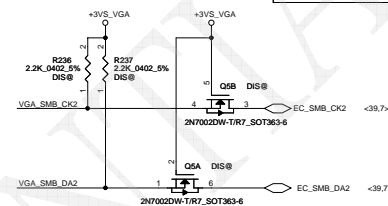
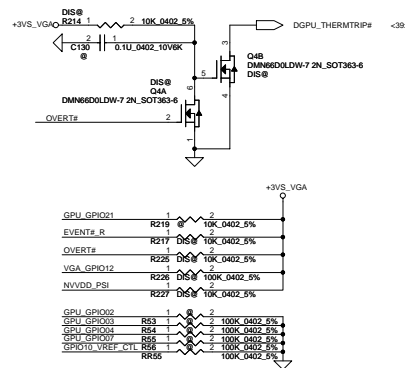
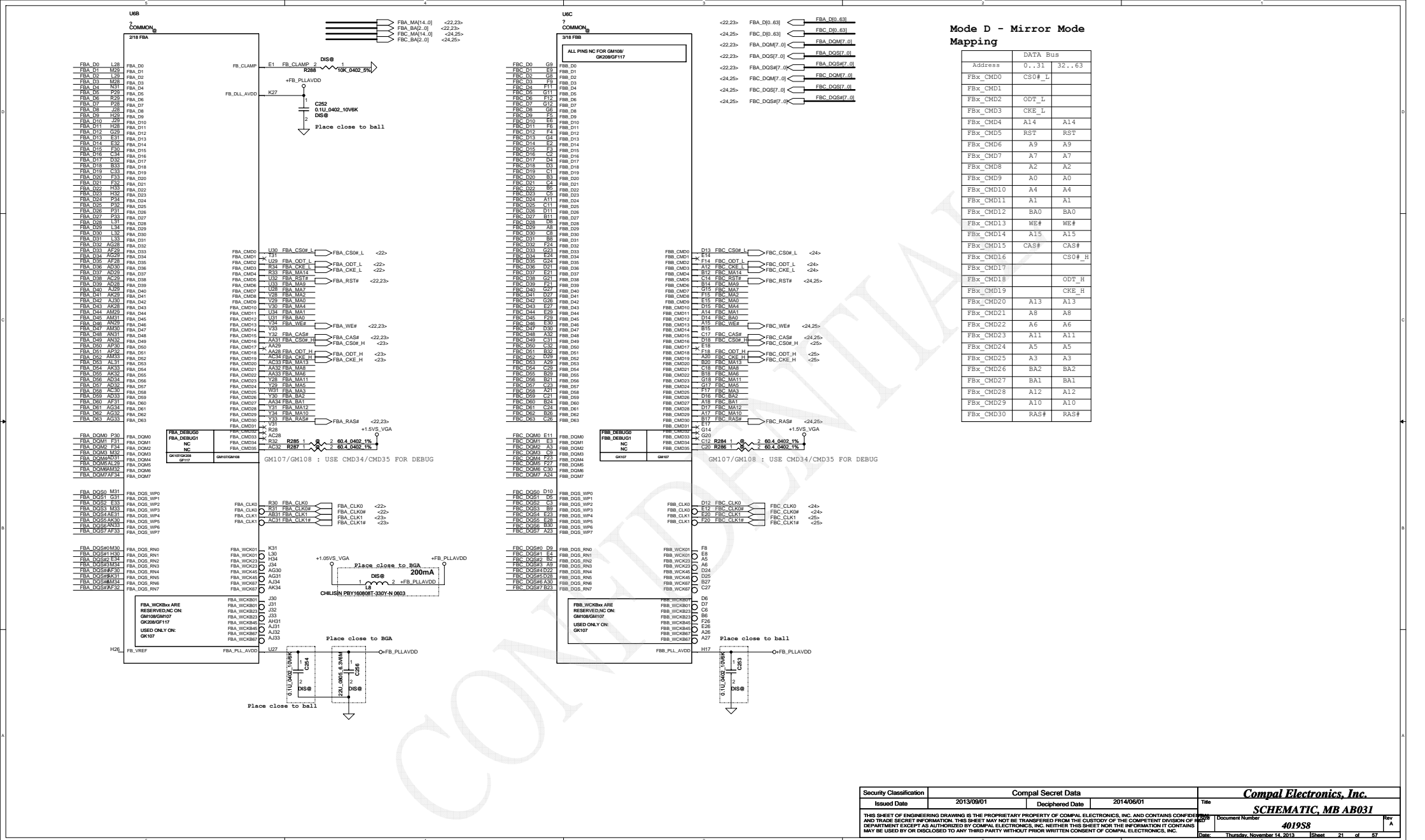


Table 12-1. GB2B-64 and GB4B-128 GPIO Description

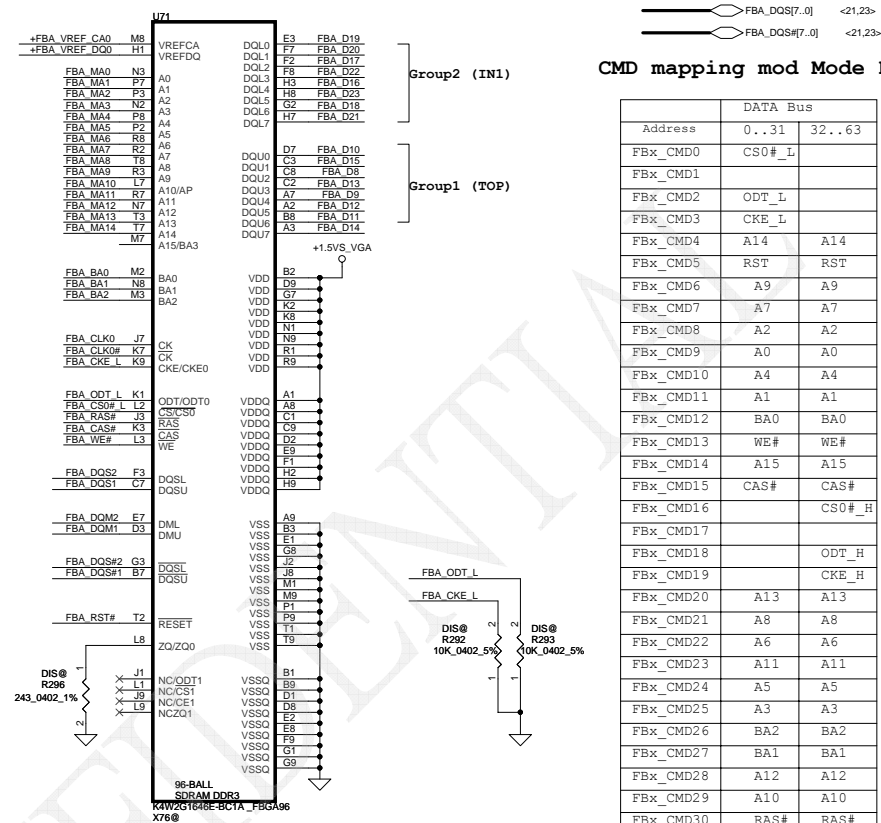
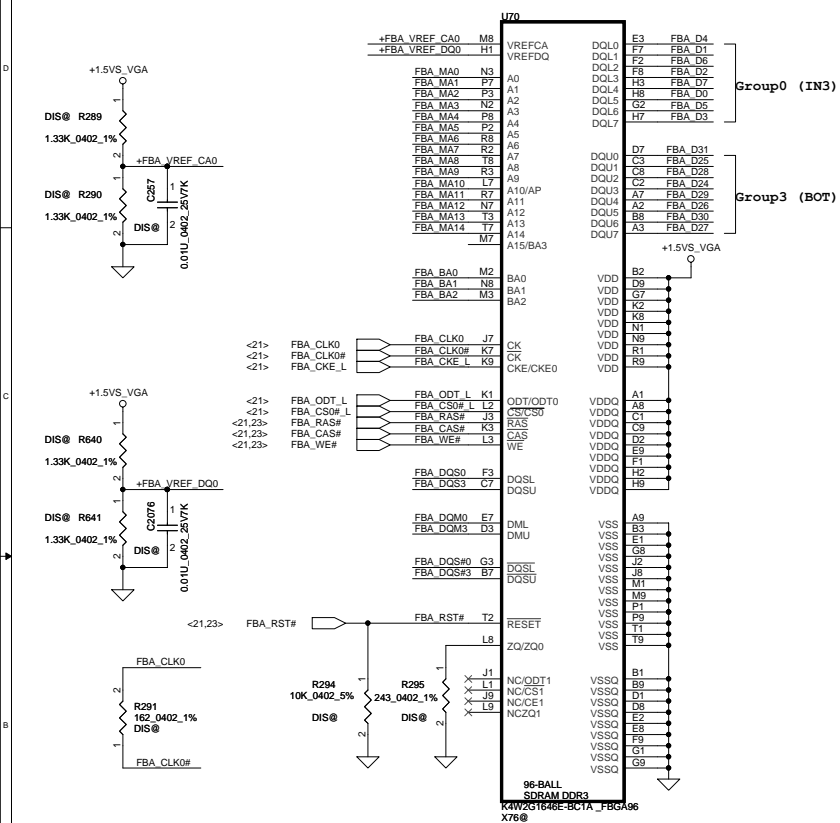
Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp Monitor for GC6 1.0	
	GC6_FB_EN	I	FB Enable for GC6 2.0	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID; pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BW_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100K pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	
GPIO5	SV3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

[VRAM Config]

GPU	Freqs	Memory Size	Memory Config	ROM_SI
W15P-GT	900 MHz	128M* 16* 8 32B	Hynix H5TC2G63FFR-11C	R329 1000 PU 4.99K
			Samsung K4W021646Q-8C1A	R332 0111 PD 45.3K
W15G-GT	900 MHz	256M* 16* 8 4GB	Micron MT41J128M16JT-09G3	R332 0110 PD 34.9K
			Micron MT41J256M16HA-09G3	R332 0101 PU 30K
W15G-GT	900 MHz	256M* 16* 8 4GB	Samsung K4W041648D-HC1A	R332 0011 PD 20K
			Hynix H5TC4G63AFR-11C	R332 0001 PD 10K

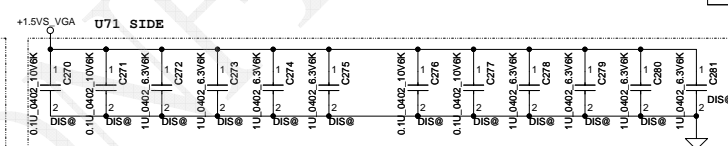
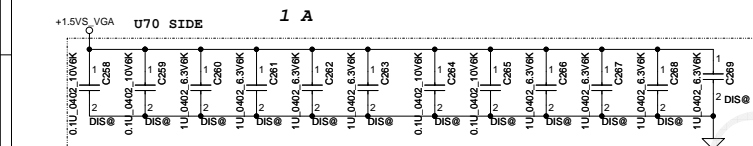


### Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

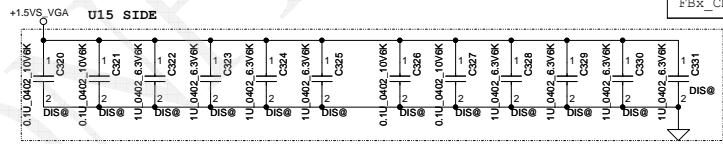
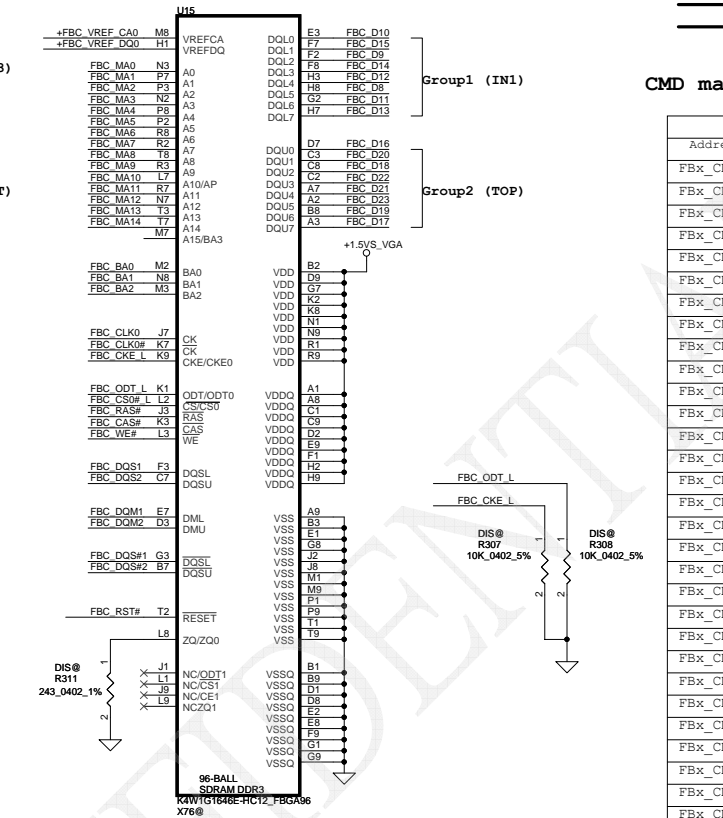
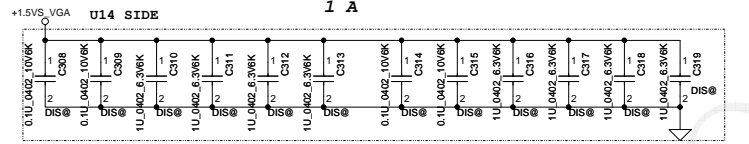
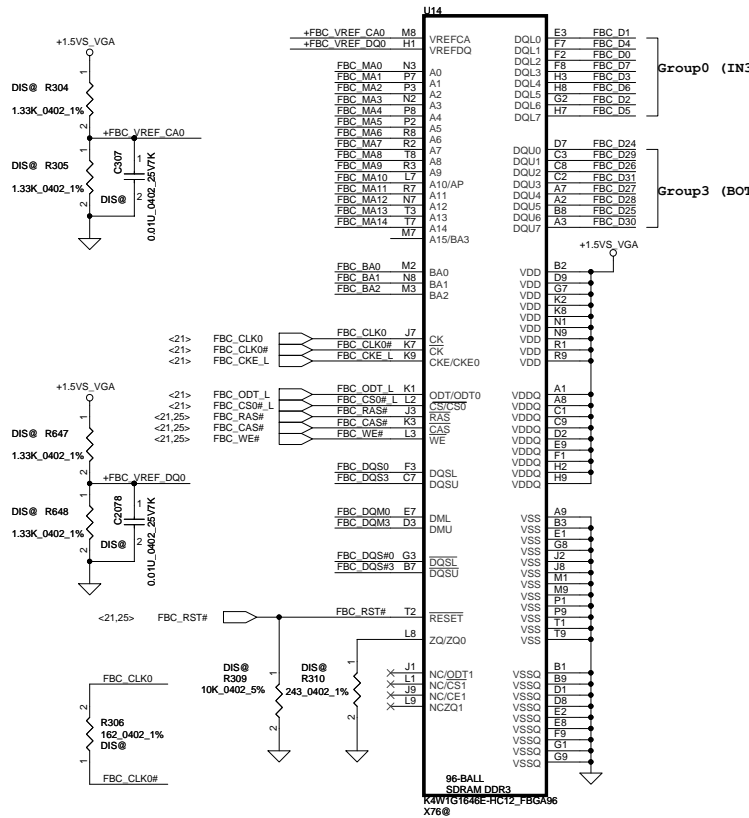
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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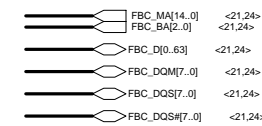
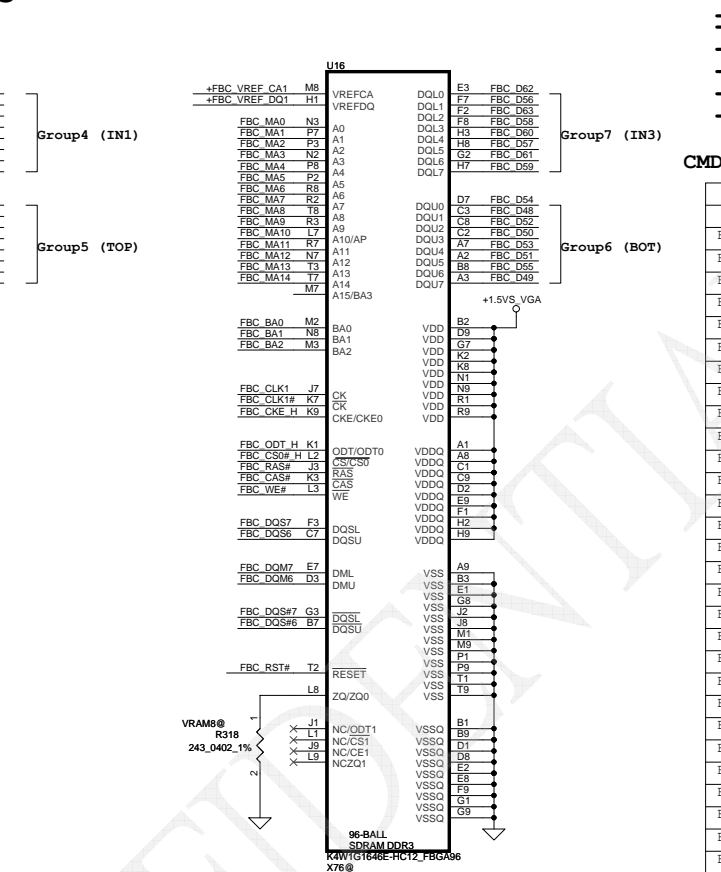
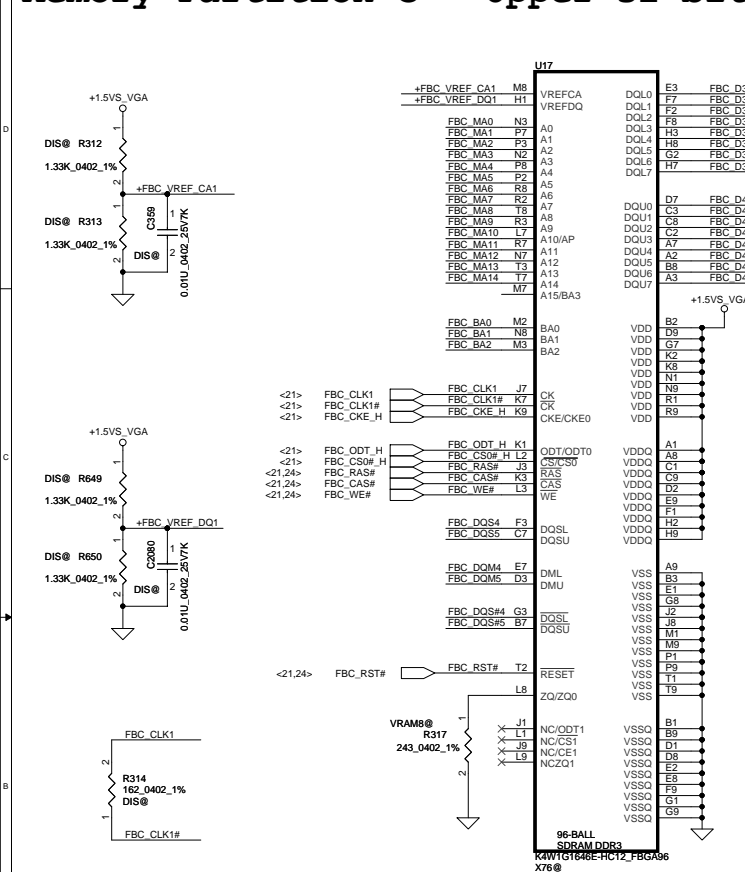


Memory Partition C - Lower 32 bits



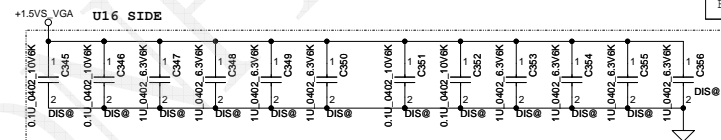
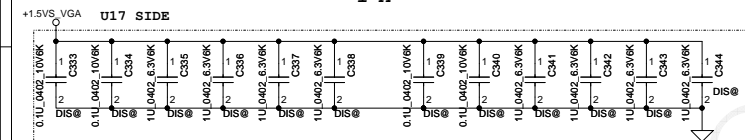
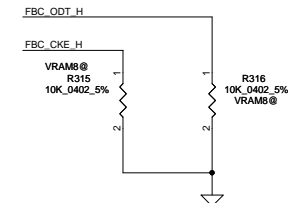


### Memory Partition C - Upper 32 bits



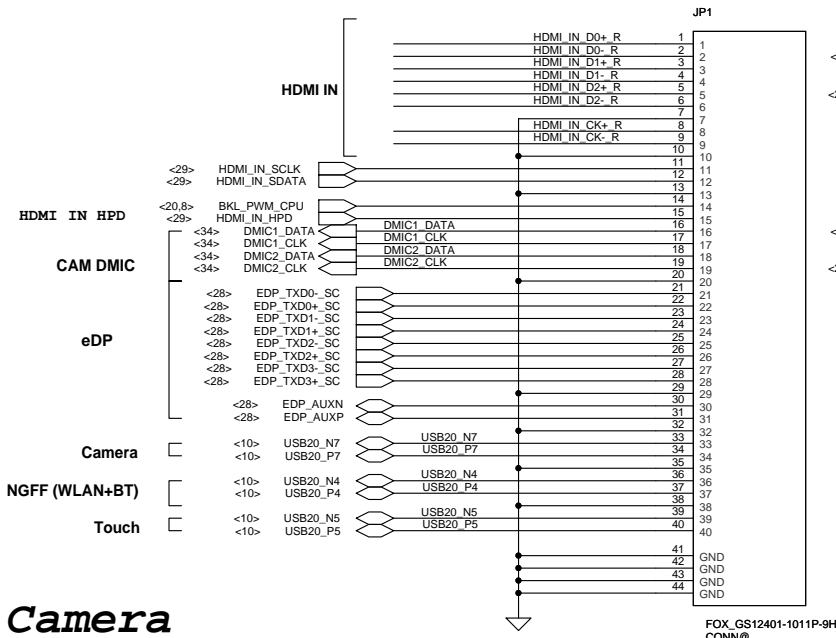
CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_F
FBx_CMD19		CKE_F
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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GND : 8 pin



Camera

Pin Layout	
1	D+
2	D-
3	VCC 3.3V
4	MIC-DAT_MAIN
5	MIC-DAT_REF
6	MIC-CLK_MAIN
7	GND
8	MIC-CLK_REF

For INTEL NFC

For BROCOM NFC

## NFC

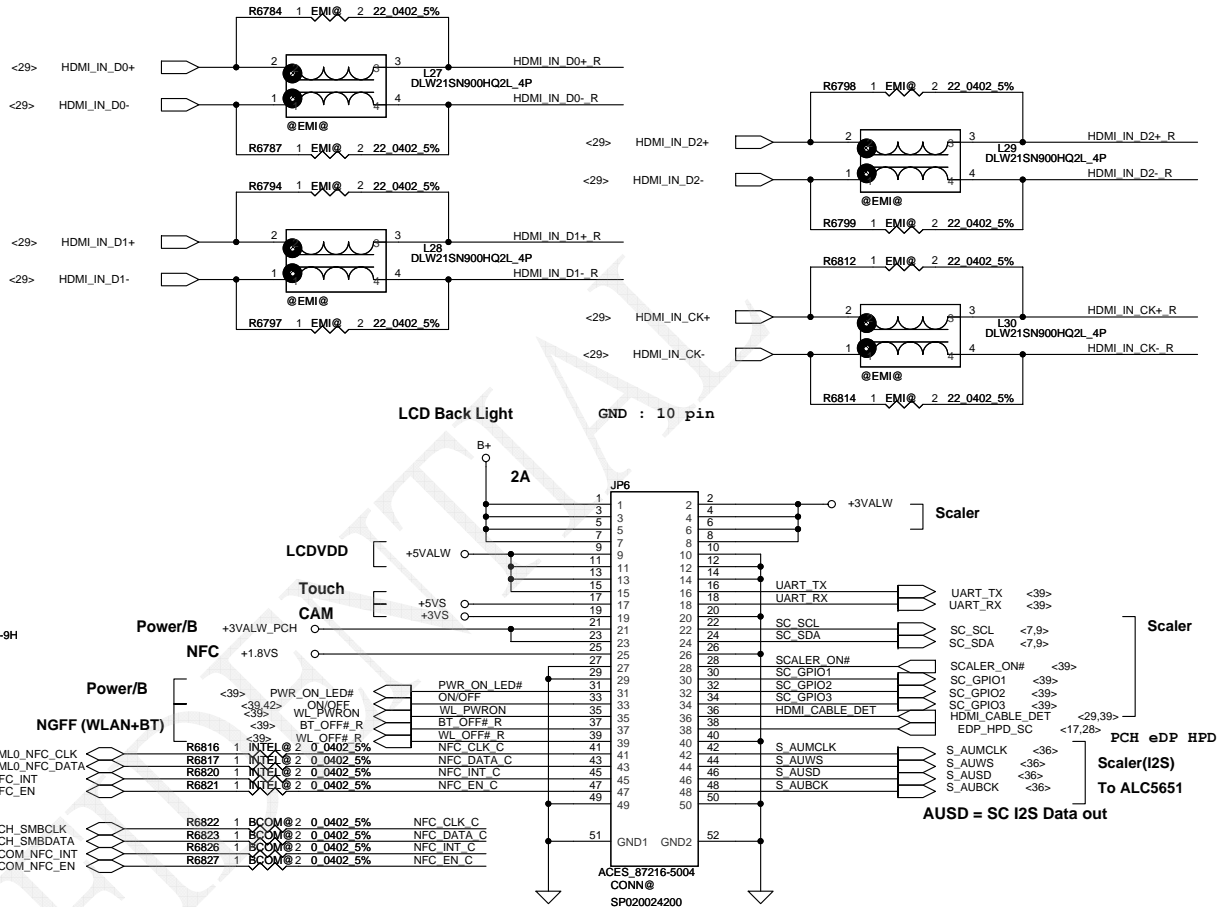
### Pin definition

Pin	Symbol	I/O	Note
1	VBAT	Input	Power supply from battery (2.8V - 5.5V)
2	VDDIO	Input	Power supply to I/O (1.62V - 3.6V)
3	I <sup>2</sup> C -SDA	I/O	BSC Serial Data Line, active low
4	I <sup>2</sup> C -SCL	I	BSC Serial Clock
5	GND	G	Ground
6	IRQ-NFC	O	BSC request, active high (Host_Wake)
7	NFC PRESENCE	G	Ground
8	REG_UP	I	NFC Power-on
9	VDD_Ext_SE	Output	Power supply to External Secure Element (1.8V or 3.0V)
10	UIM_PWR	Input	Power supply to UICC (1.78V - 3.3V)
11	SWP	I	SWP I/O 0 (Single-Wire Protocol interface)
S1	GND	G	Ground
S2	GND	G	Ground

Remark: The connector is bottom conduct with golden plating of FPC cable

### Pin definition

Pin	Symbol	I/O	Note
1	TX2	I/O	Coil output 2
2	GND	G	Ground
3	TX1	I/O	Coil output 1
S1	GND	G	Ground
S2	GND	G	Ground



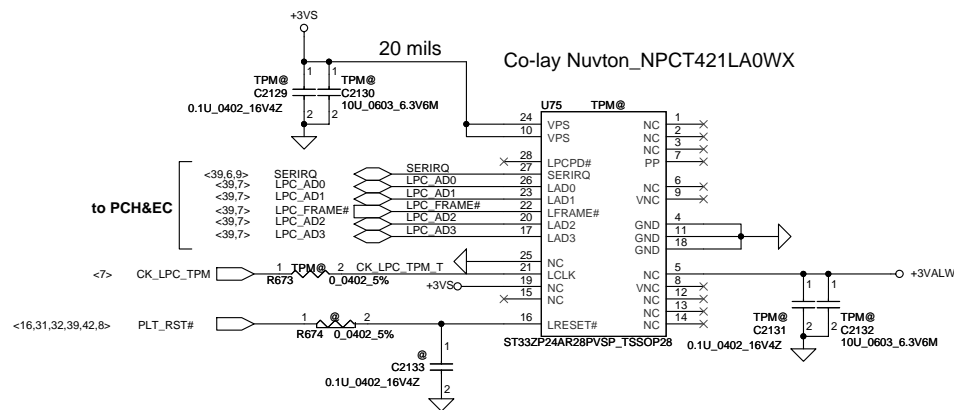
Power	Function	Current	Pin Count	Total Pin
B+	INVPWR_B+	2A	4 Pin	17 Pin
+5VALW	+LCDVDD	1.5A-2A	4 Pin	
+5VS	Touch	0.5 A	1 Pin	
+3VALW_PCH	Power/B	30 mA	2 Pin	
+3VS	NGFF (WLAN+BT)	0.6 A	2 Pin	
+3VALW	CAM	0.15 A	1 Pin	
+1.8V	Scaler	2 A	4 Pin	
	NFC	X	1 Pin	18 Pin
GND	X	X	X	

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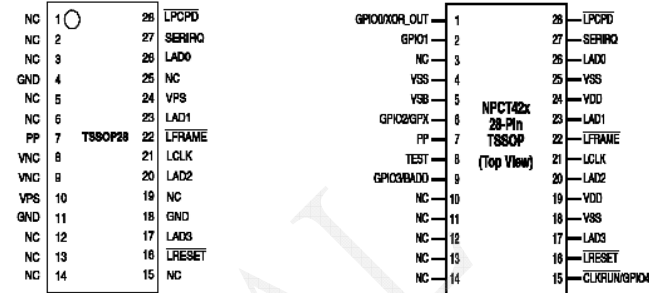
SCHEMATIC, MB AB031

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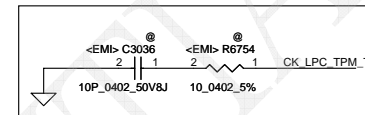


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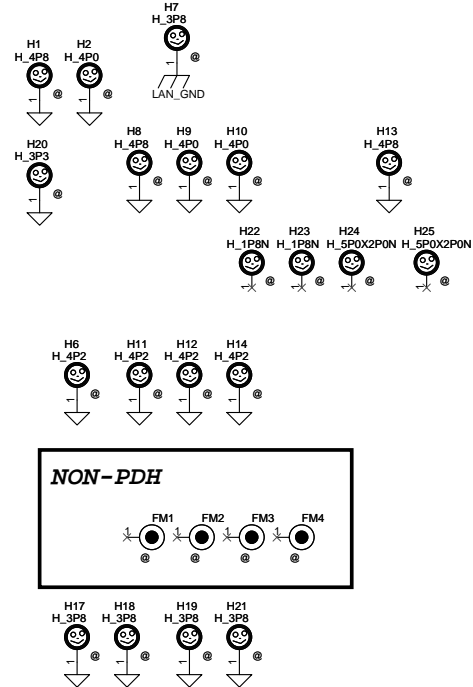
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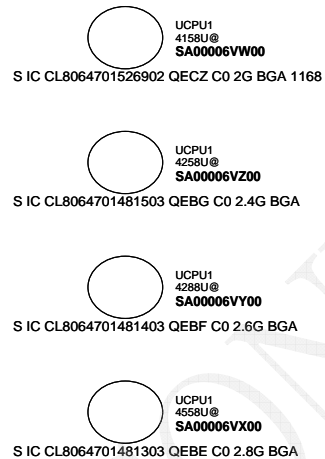
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*Screw*



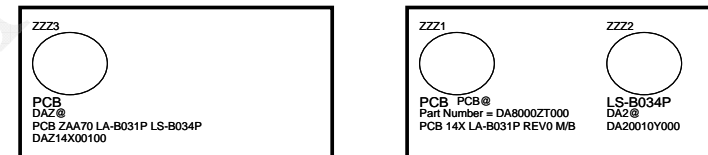
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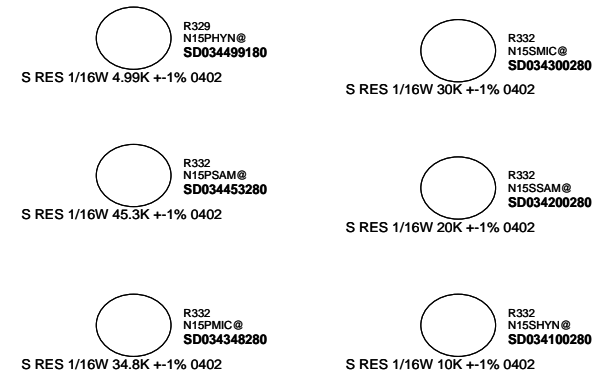
## GPU



## ISPD



## VRAM



GPU	Freq.	Memory Size	Memory Config	ROM_Si
A740			Hynix H5TC2G63FFR-11C	R329 1000 PU 4.99K
N159-GT	900 MHz	128M* 16' 8 2GB	Samsung K4W2G1646Q-BC1A	R332 0111 PD 45.3K
			Micron MT41J128M16JT-093G	R332 0110 PD 34.8K
A540			Micron MT41J256M16HA-093G	R332 0101 PU 30K
N159-GT	900 MHz	256M* 16' 4 2GB	Samsung K4W4G1646D-HC1A	R332 0011 PD 20K
			Hynix H5TC4G63AFR-11C	R332 0001 PD 10K

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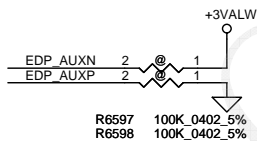
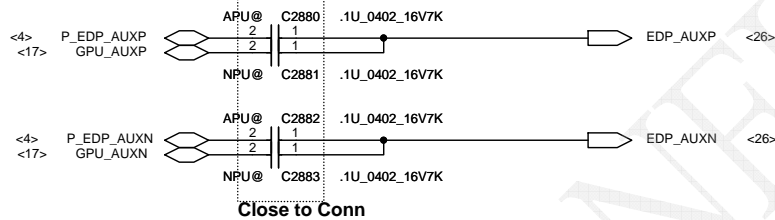
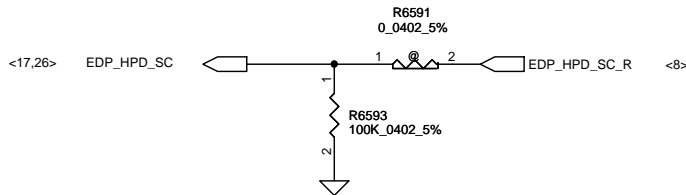
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DIS only

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<17>	VGA_EDP_SC_TX1+	NPU@ C2856	2	1	.1U_0402_16V7K	EDP_TXD1+ SC
<17>	VGA_EDP_SC_TX2-	NPU@ C2858	2	1	.1U_0402_16V7K	EDP_TXD2- SC
<17>	VGA_EDP_SC_TX2+	NPU@ C2860	2	1	.1U_0402_16V7K	EDP_TXD2+ SC
<17>	VGA_EDP_SC_TX3-	NPU@ C2862	2	1	.1U_0402_16V7K	EDP_TXD3- SC
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UMA only

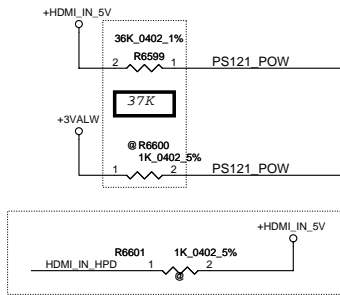
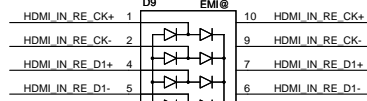
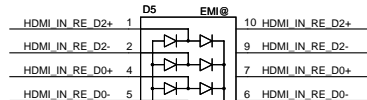
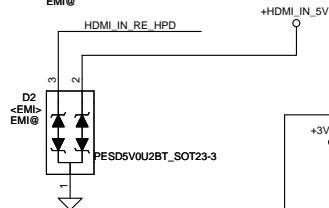
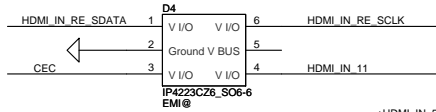
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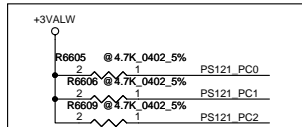
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## HDMI IN

DVT Change symbol of D4 to SC300001100(EMI Suggest)



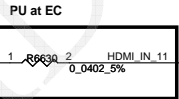
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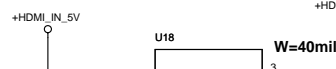
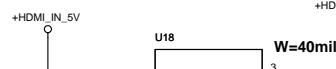
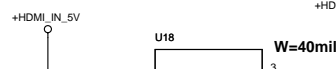
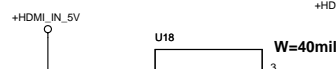
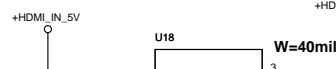
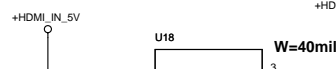
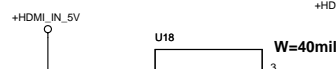
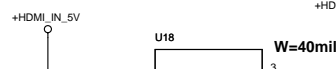
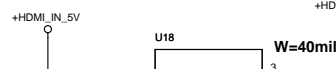
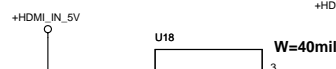
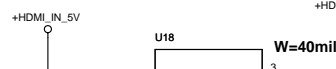
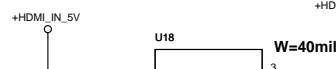
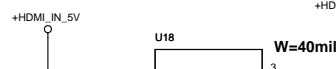
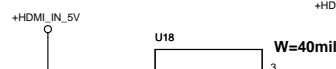
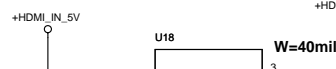
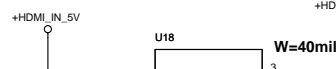
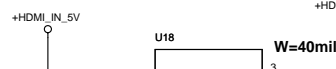
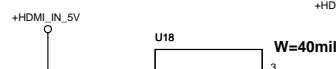
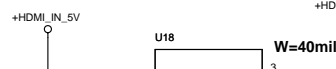
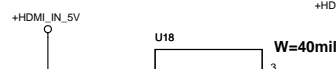
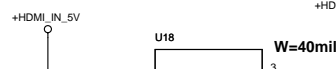
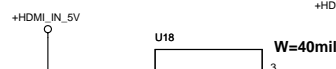
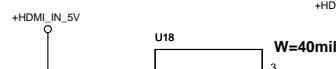
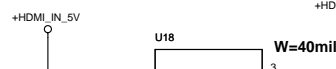
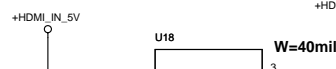
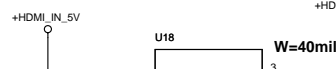
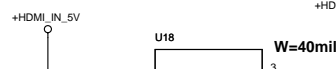
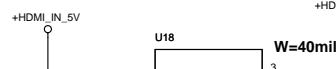
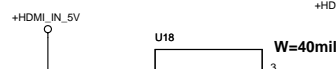
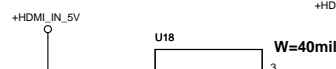
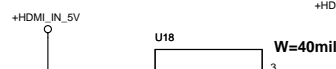
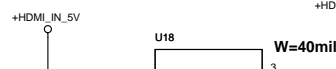
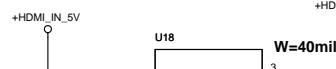
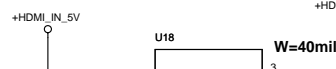
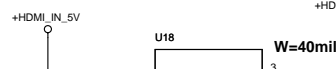
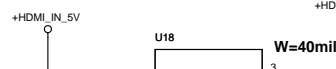
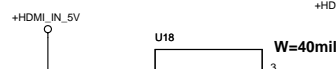
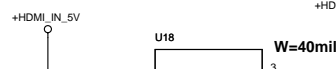
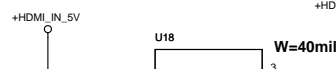
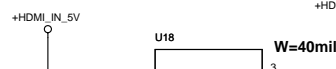
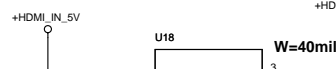
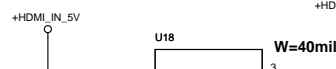
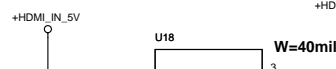
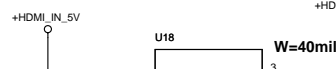
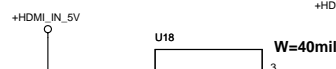
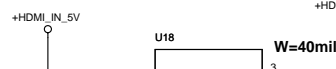
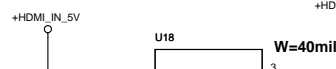
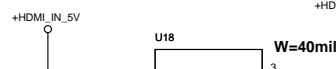
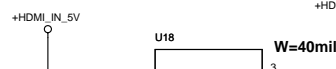
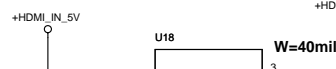
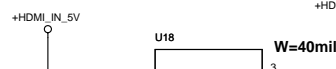
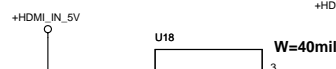
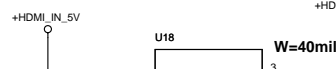
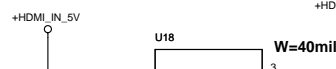
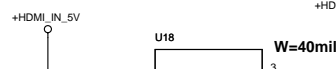
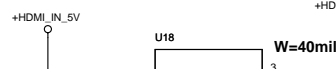
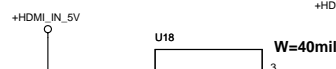
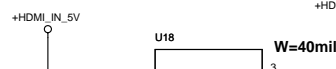
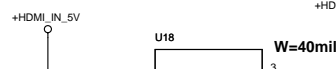
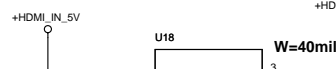
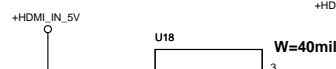
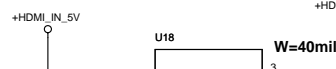
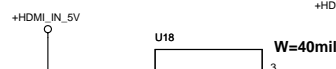
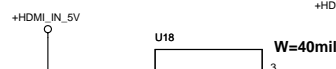
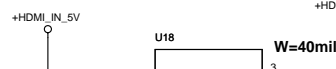
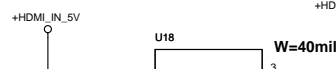
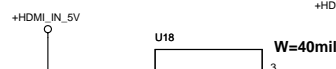
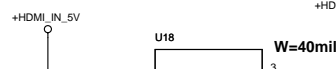
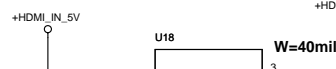
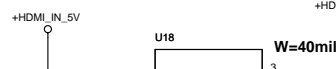
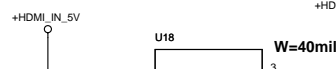
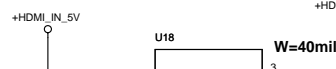
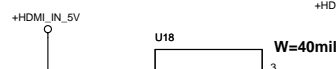
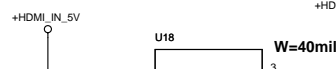
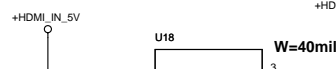
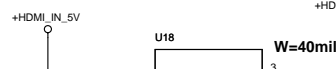
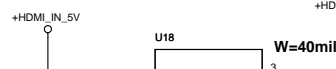
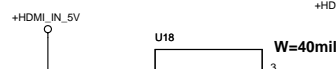
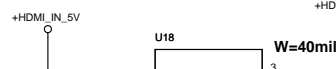
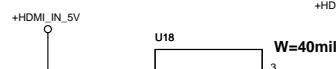
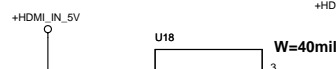
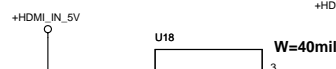
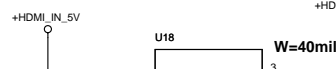
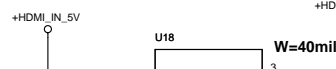
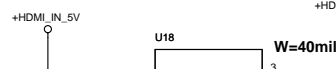
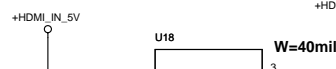
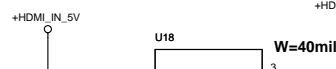
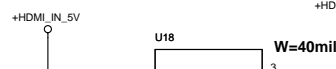
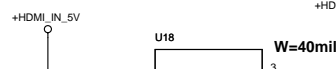
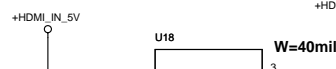
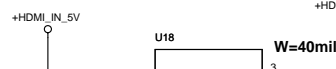
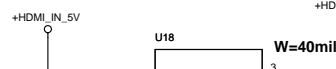
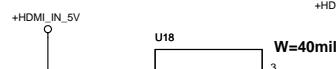
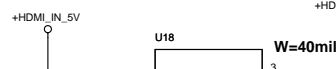
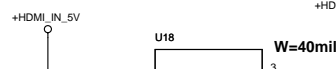
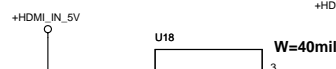
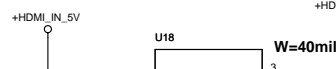
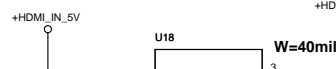
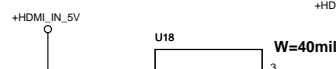
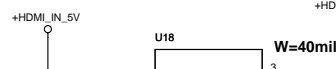
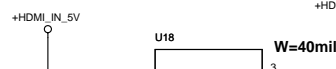
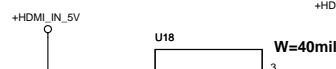
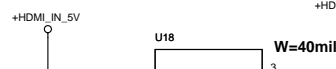
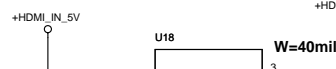
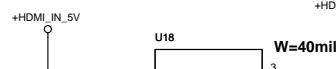
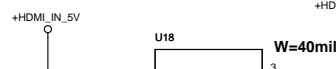
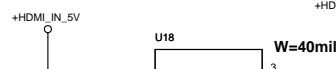
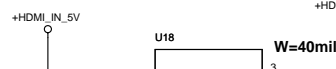
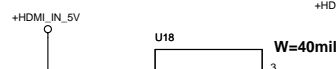
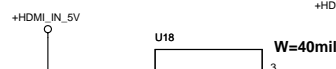
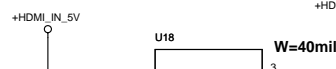
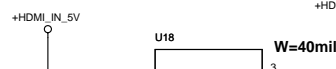
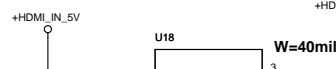
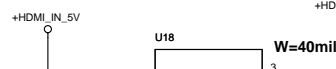
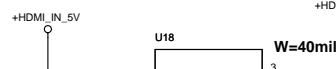
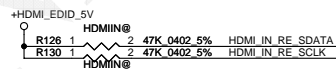
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[PC2,PC1,PC0]=010, 10dB  
[PC2,PC1,PC0]=011, 7dB  
[PC2,PC1,PC0]=100, 1.5dB  
[PC2,PC1,PC0]=101, 4dB  
[PC2,PC1,PC0]=110, 9dB  
[PC2,PC1,PC0]=111, 7dB

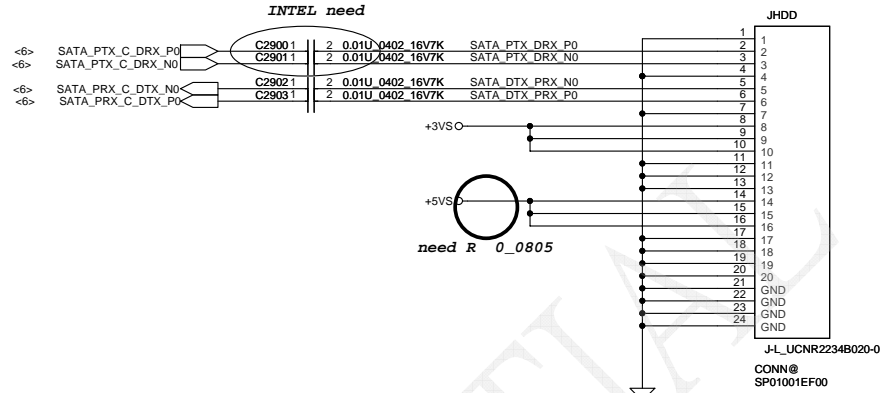
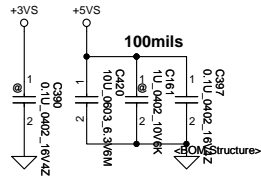
HDMI\_CABLE\_DET



### PU at EC

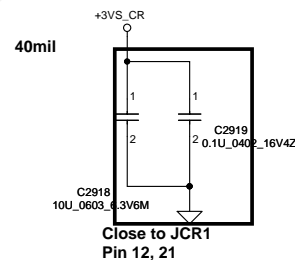
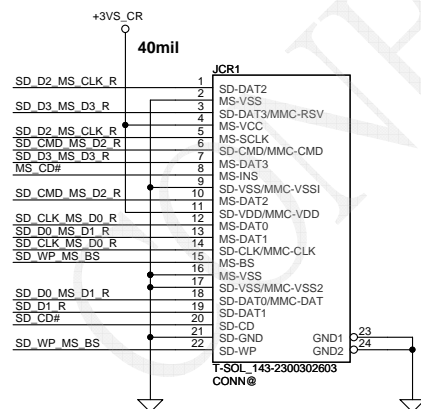
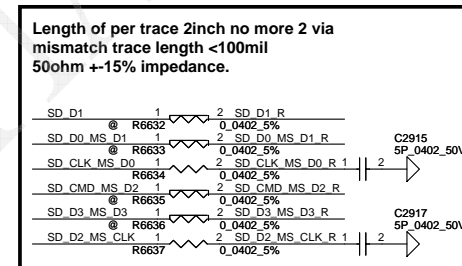
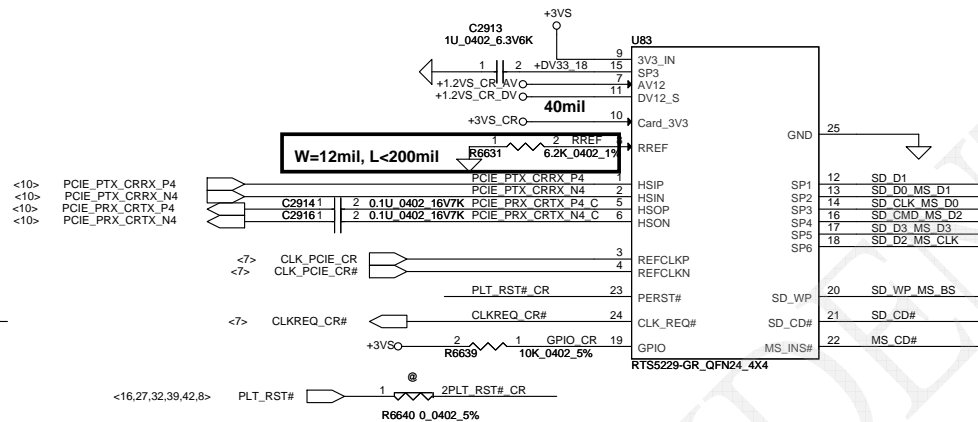
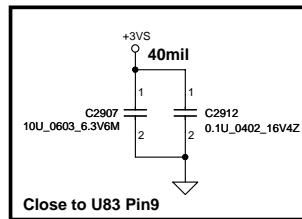
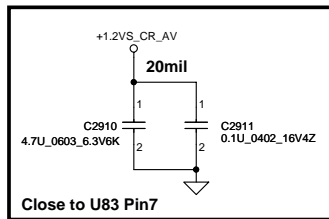
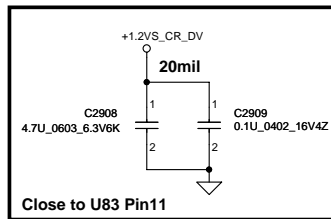


HDD

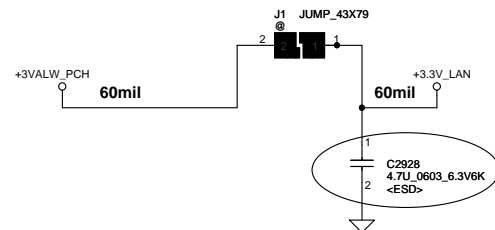


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				Date:	Thursday, November 14, 2013
				Sheet	30 of 57
				Rev	A

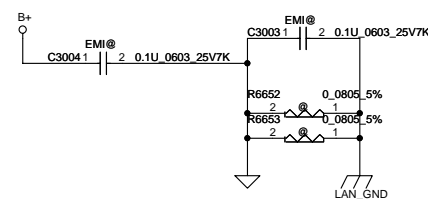
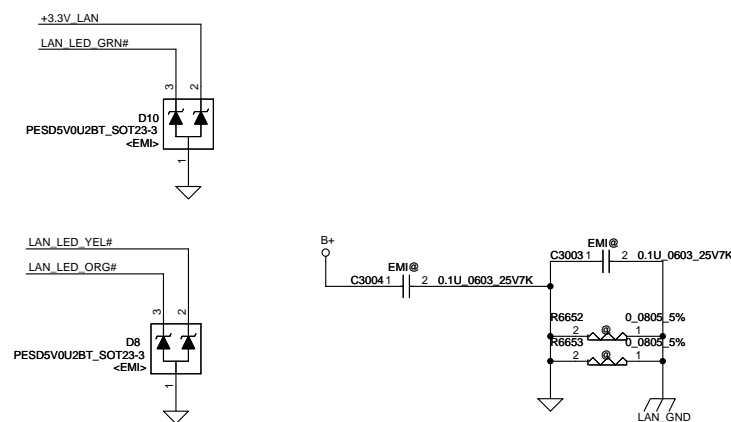
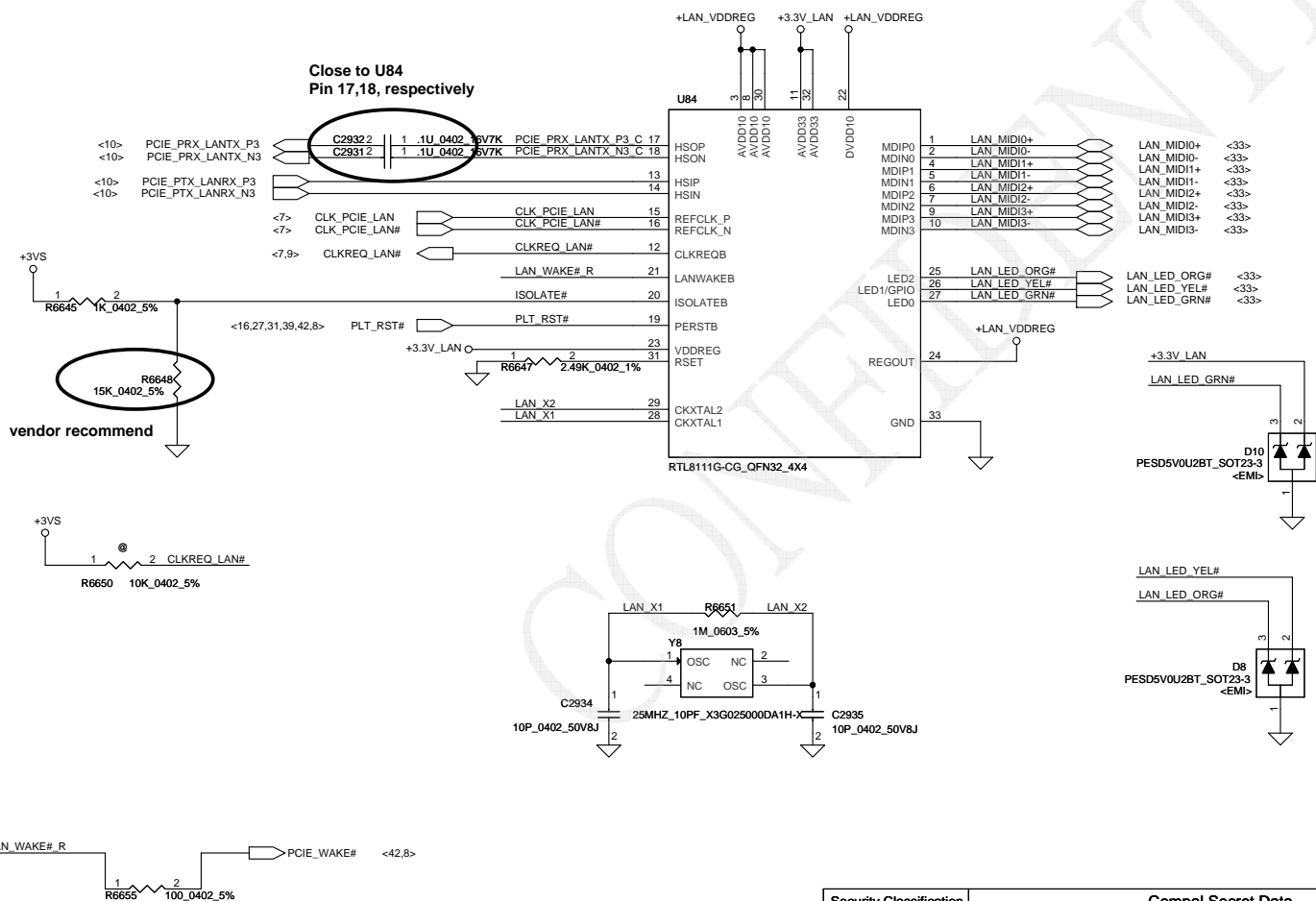
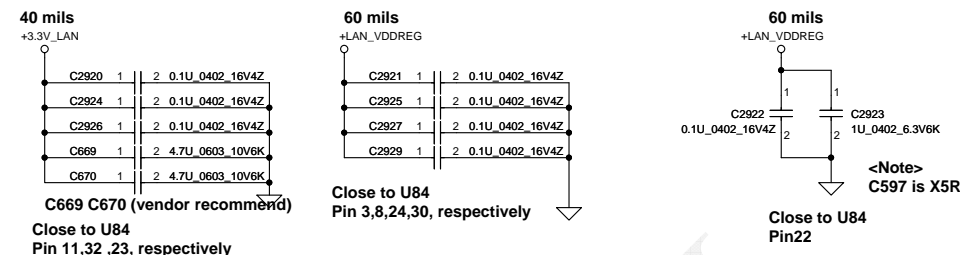


# WOL circuit (Connect +3V\_LAN to +3VALW)



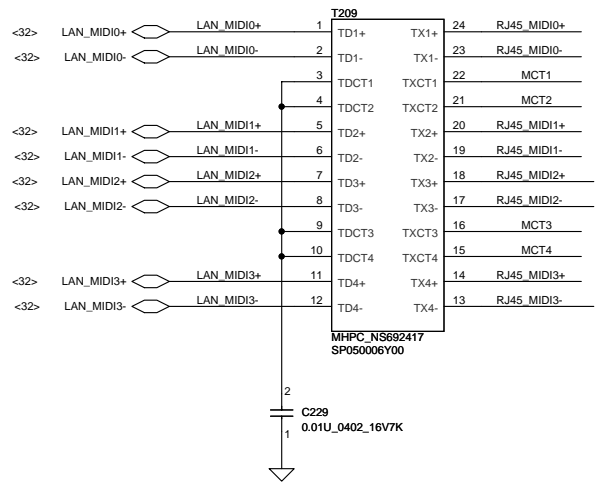
+3.3V\_LAN rising time (10%~90%) need > 0.5ms and <100ms.

# Power ( Decoupling Cap. )



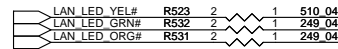
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Issued Date	2011/09/12	Deciphered Date	2012/09/12	2012/09/12
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Compal Electronics, Inc.				Document Number
SCHEMATIC, MB AB031				4019S8
Date: Thursday, November 14, 2013				Sheet 32 of 57





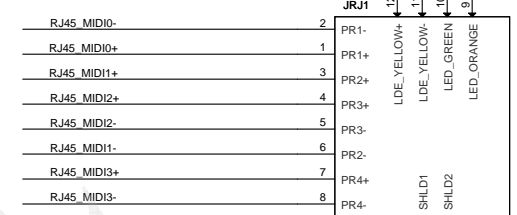
Yellow  
Green / Orange

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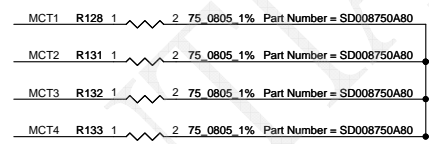


20mils

LAN Connector

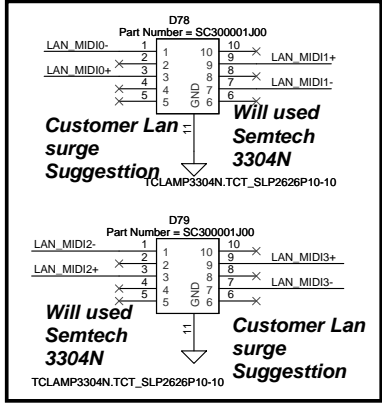
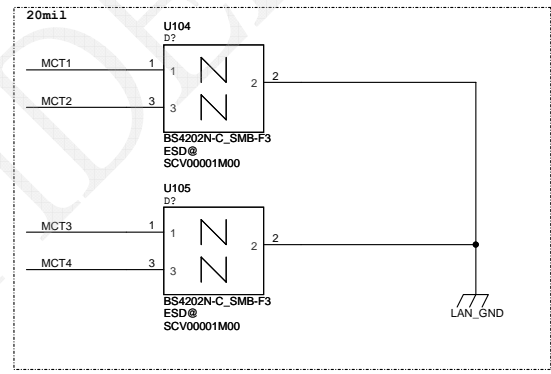


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CONN@  
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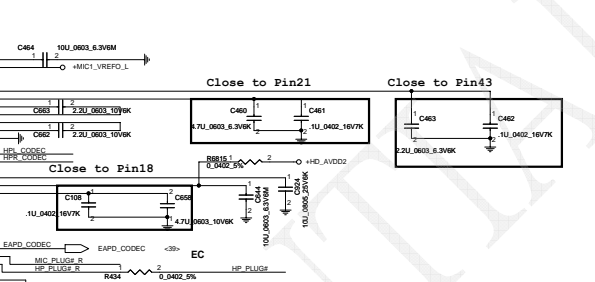
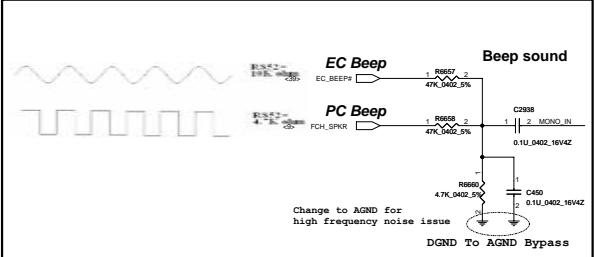
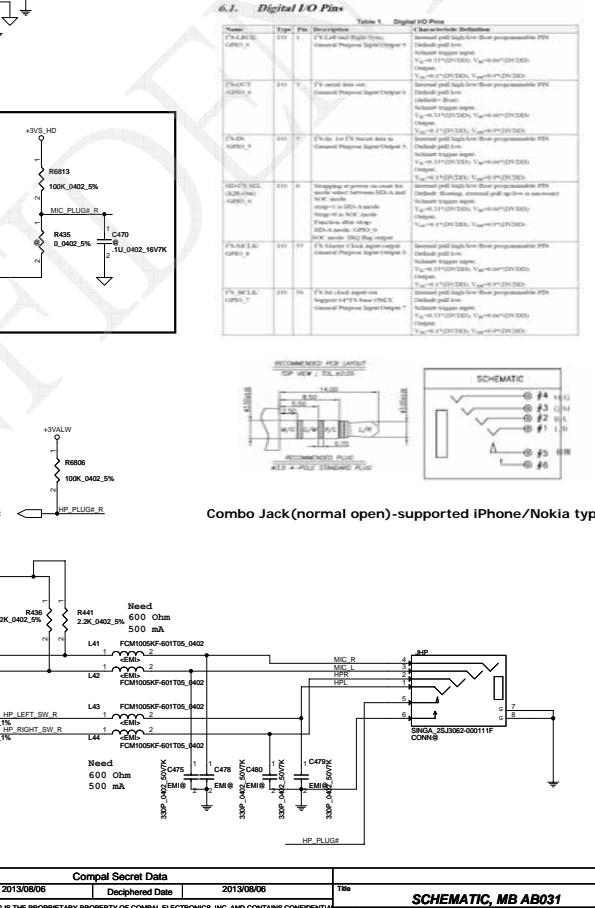


40mil

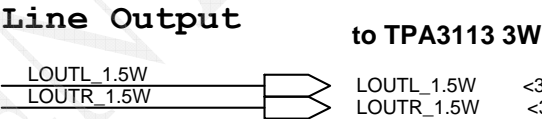
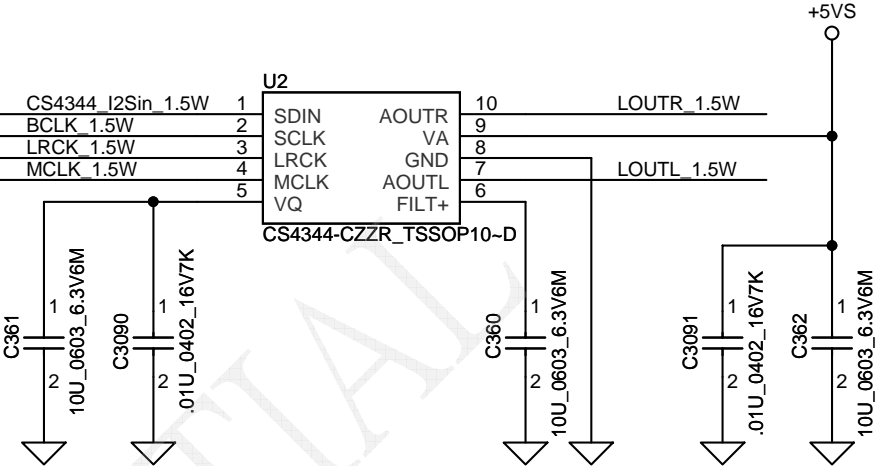
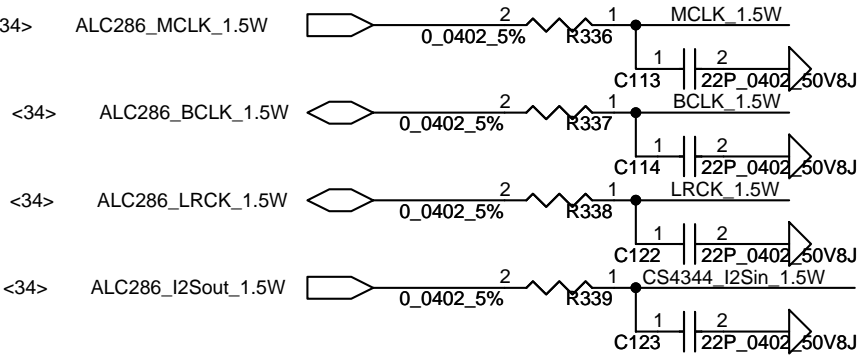
10P 2KV J NPO 1206 H1.25  
Part Number = SE00000U000



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[illegible]

From ALC286 I2S1 Interface (from ALC286)



Pin Name	#	Pin Description
SDIN	1	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
DEM/SCLK	2	De-Emphasis/External Serial Clock Input (Input) - used for de-emphasis filter control or external serial clock input.
LRCK	3	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters.
VQ	5	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.
FILT+	6	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
AOUTL	7	Left Channel Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.
GND	8	Ground (Input) - ground reference.
VA	9	Analog Power (Input) - Positive power for the analog and digital sections.
AOUTR	10	Right Channel Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.

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## PC/HDMI SPK Switch

CH1: ALC286  
CH2: ALC5651

C2978 0.22U\_0402\_10V6K  
C370 1U\_0402\_6.3V6K  
C2979 0.22U\_0402\_10V6K  
C371 1U\_0402\_6.3V6K

C2977 1U\_0603\_25V6K

U90

NC1 NO1

COM1

NC2 NO2

COM2

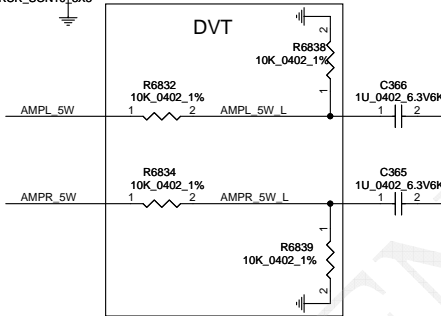
IN1 IN2

GND TP

TS5A22364DRCR\_SON10\_3X3

0:PC MODE  
1:HDMI MODE

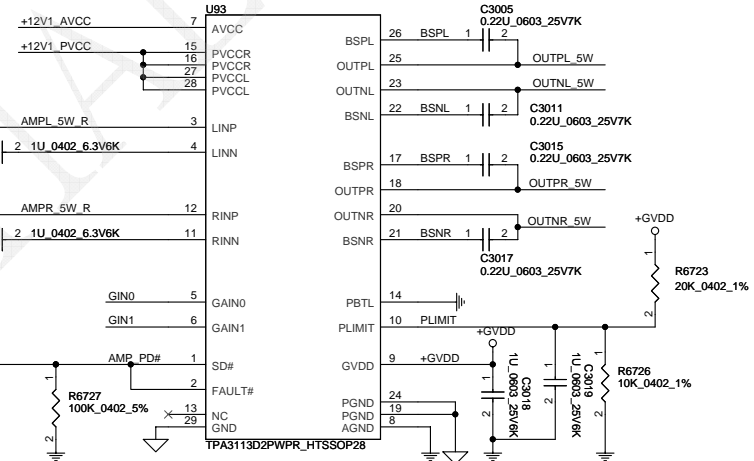
@ R6712  
10K\_0402\_5%



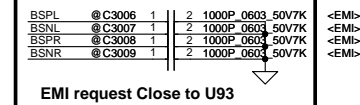
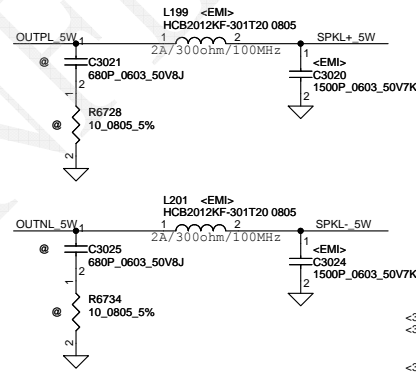
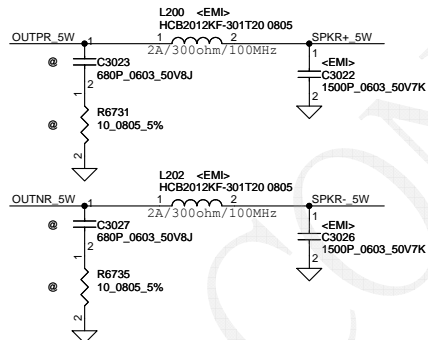
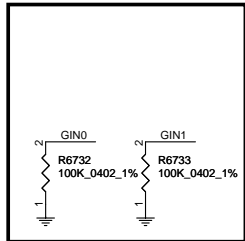
Close to U93  
Pin7

Close to U93  
Pin15,16

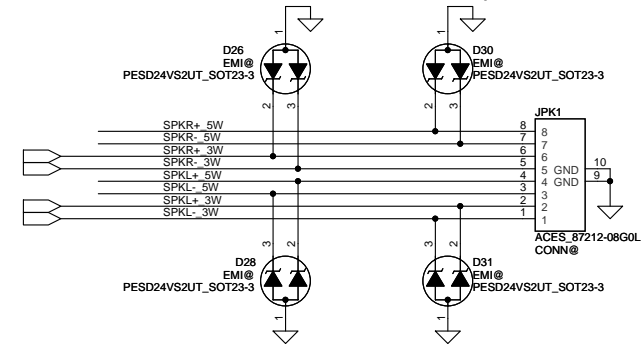
Close to U93  
Pin27,28



TPA3113 for Speaker

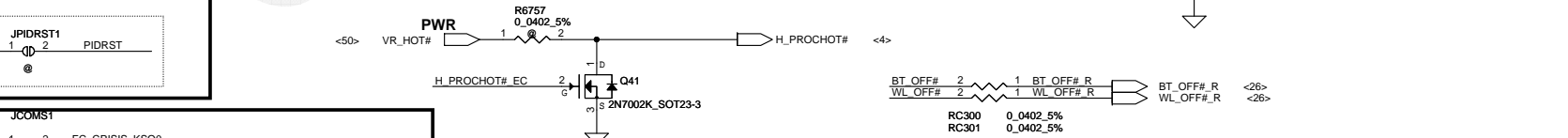
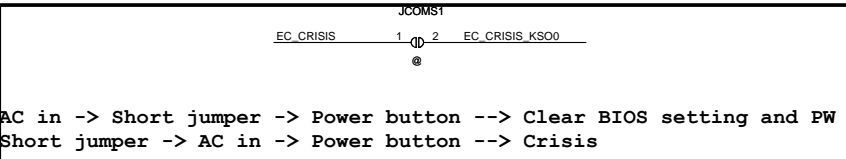
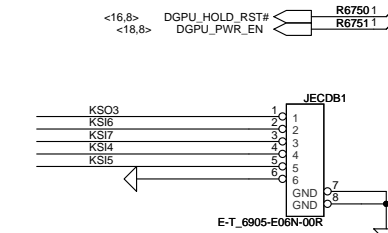
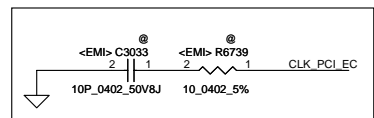


Speaker Conn.

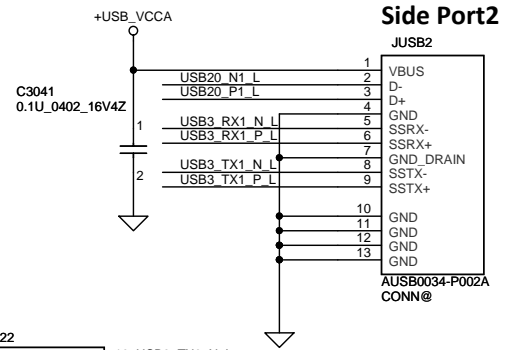
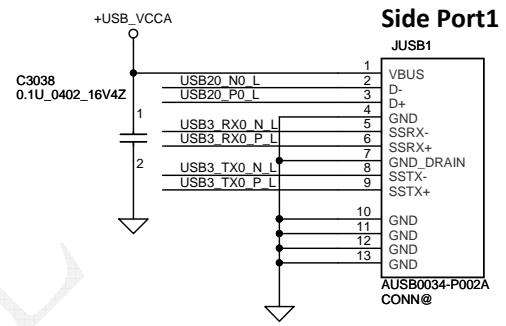
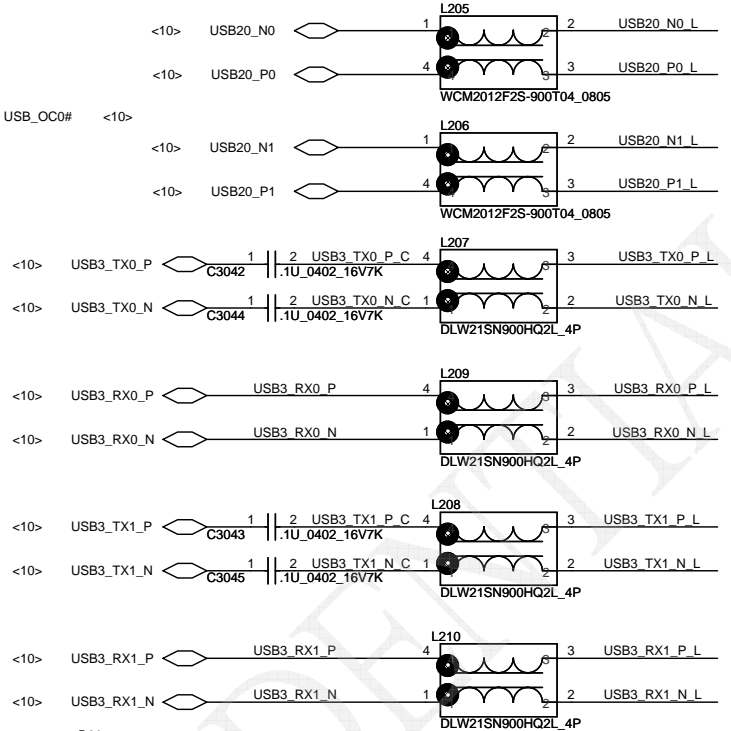
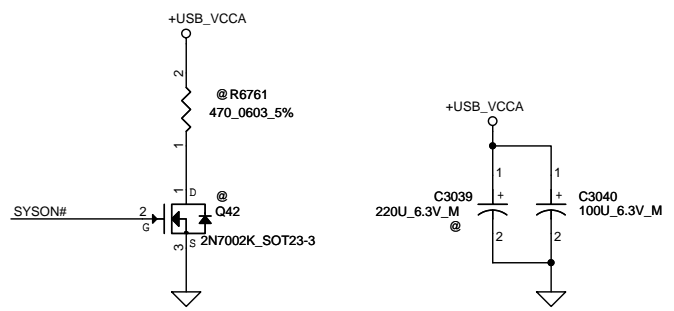
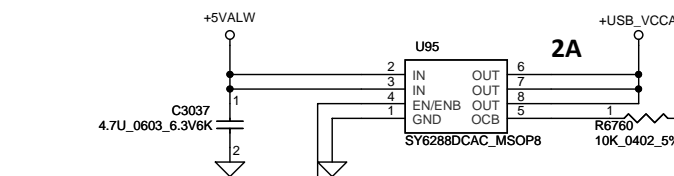


GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

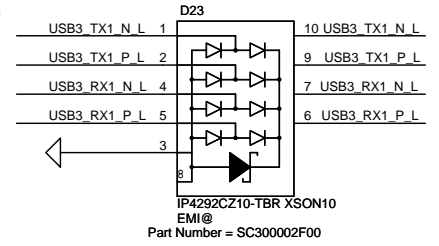
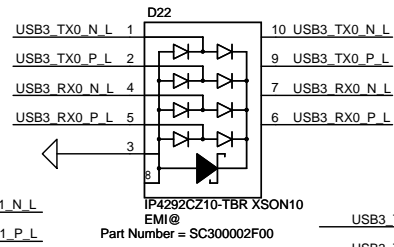
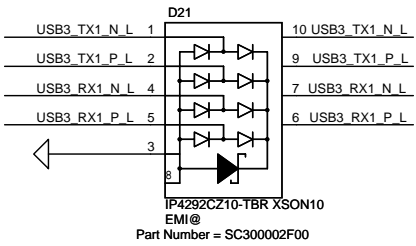
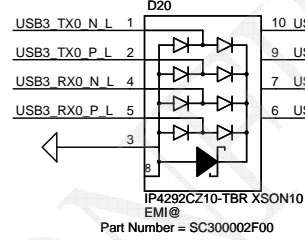
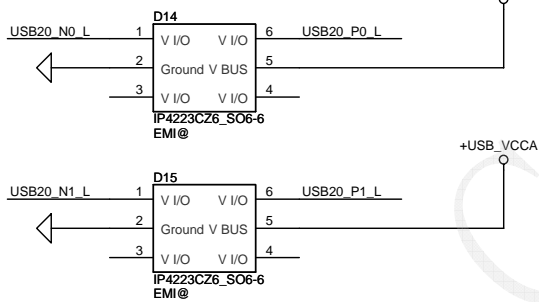
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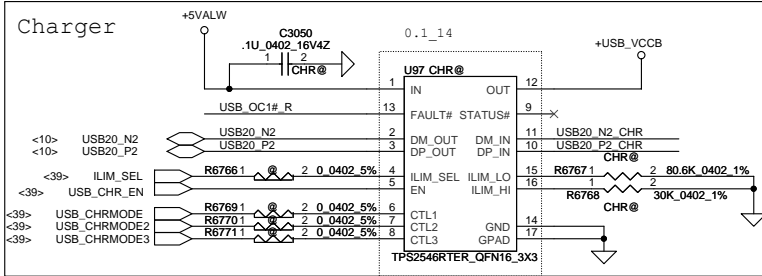
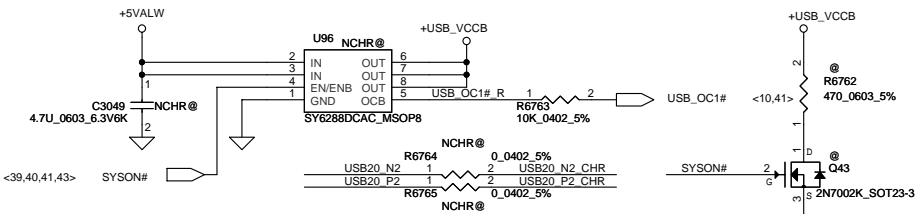


DVT Change symbol of D14/D15 to SC300001100(EMI Suggest)

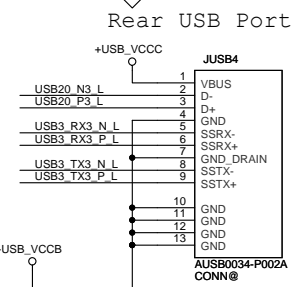
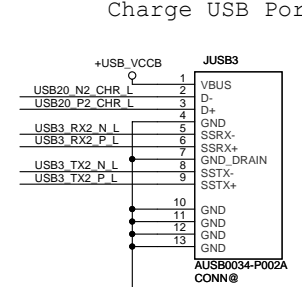
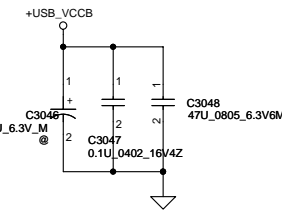
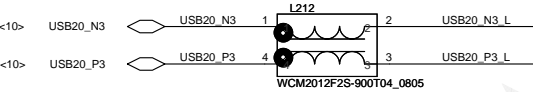
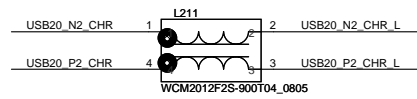
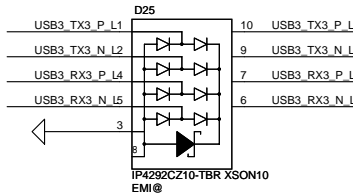
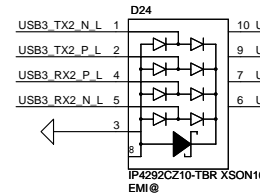
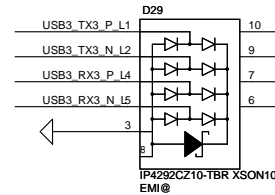
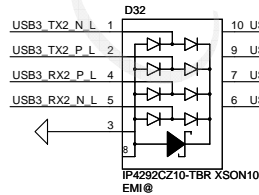
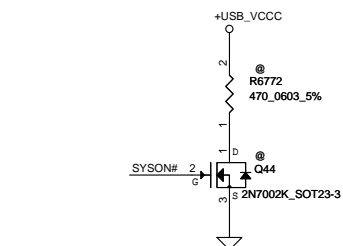
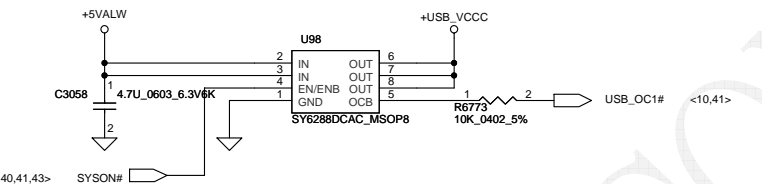


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						C	D	

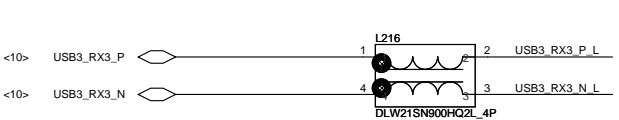
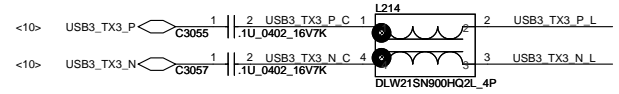
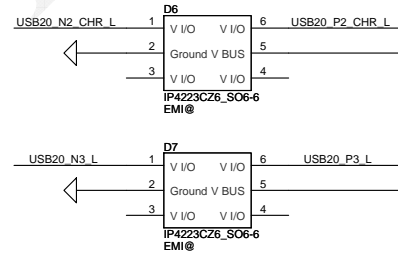




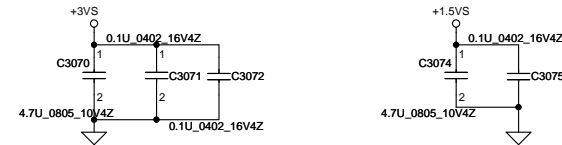
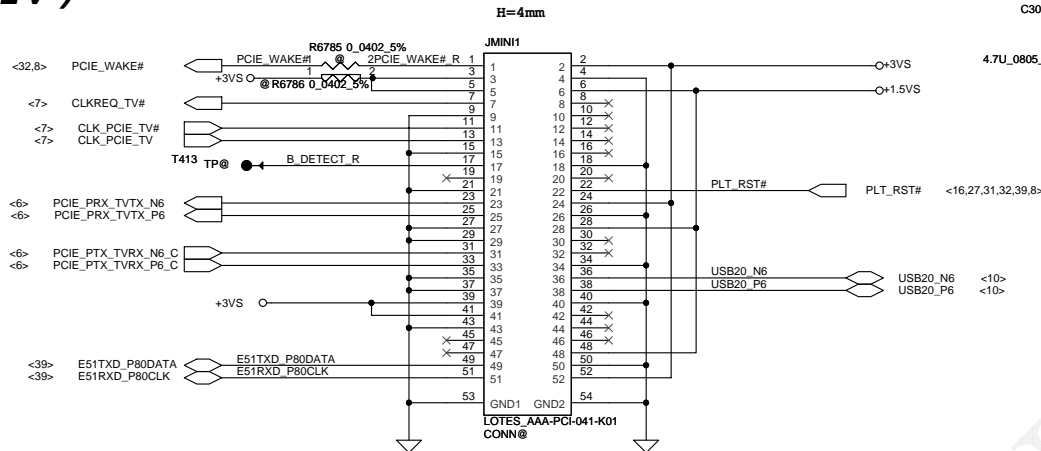
System Global Power State	TPS2546/TPS2544 Mode	Charging	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	CDP, load detection with ILIM_LO + 80mA thresholds or if a BC1.2 primary detection occurs		1	1	1	1	ILIM_HI
S4/S5	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 80 mA thresholds		0	0	1	1	ILIM_HI
S3	SDP, keyboard/mouse wake-up		0	1	0	0	ILIM_HI



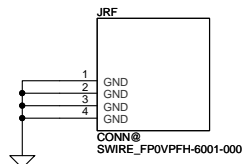
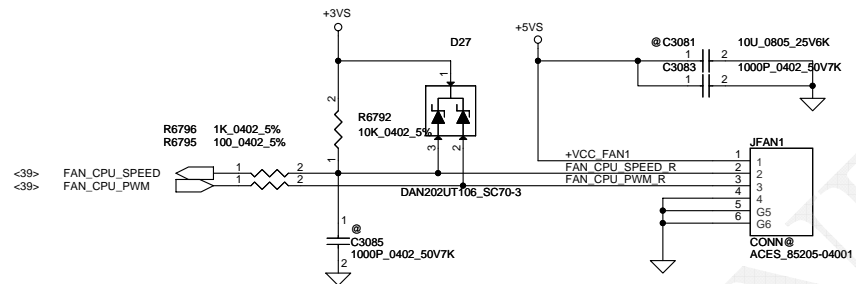
DVT Change symbol of D6/D7 to SC300001100(EMI Suggest)



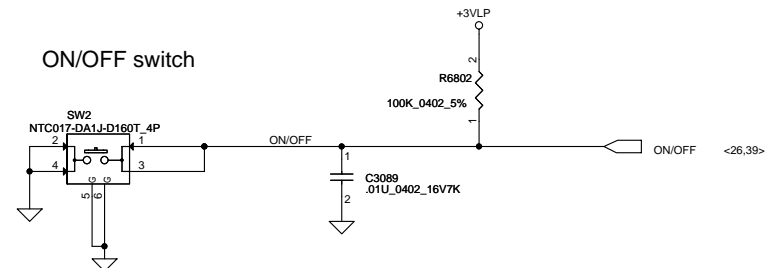
***MINI (TV)***



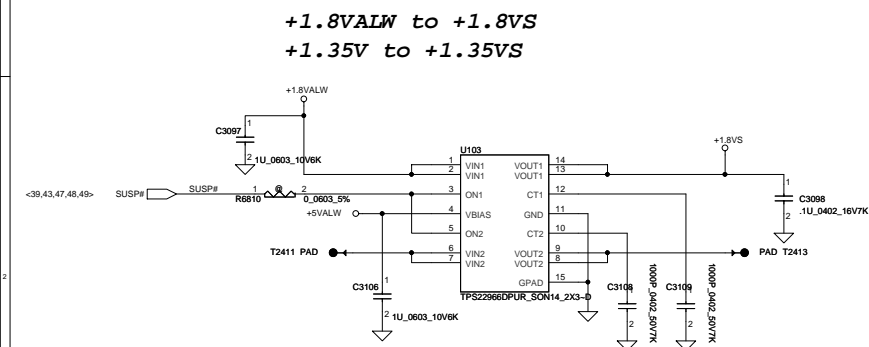
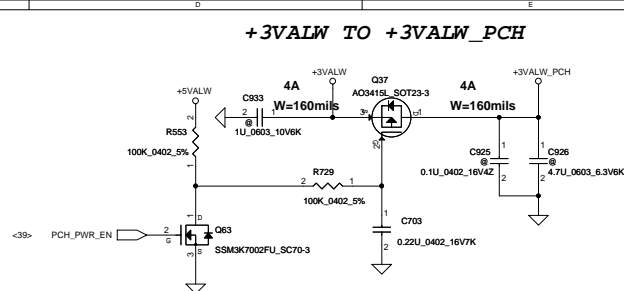
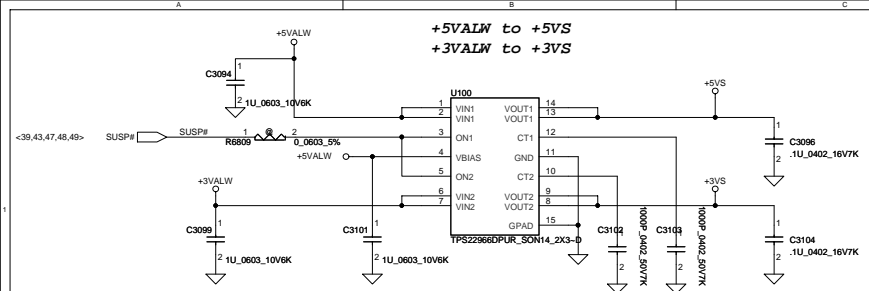
### Fan Control circuit



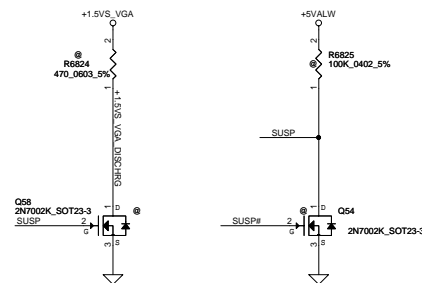
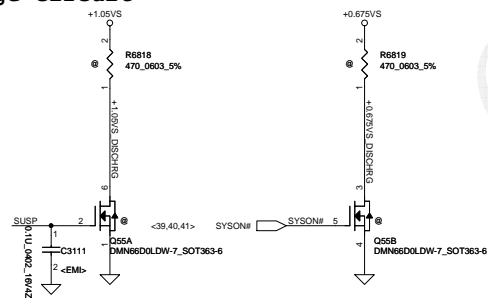
## Power Button



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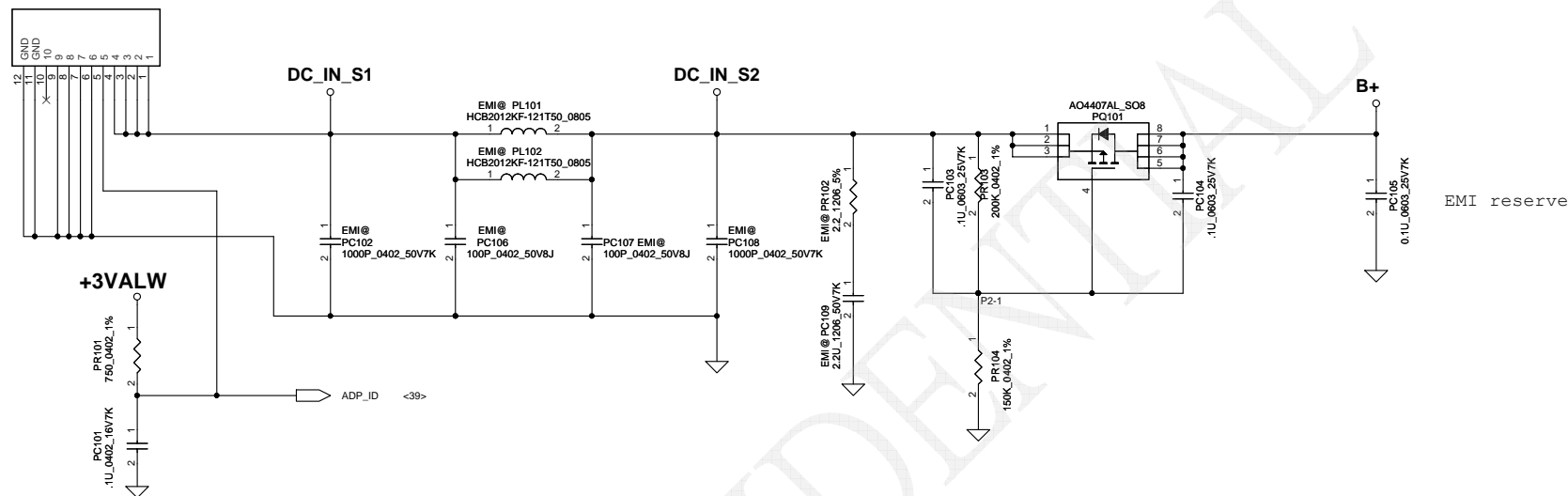
# Discharge circuit



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CONN@  
ACES\_50273-01001-001  
PJP1



+RTCBATT

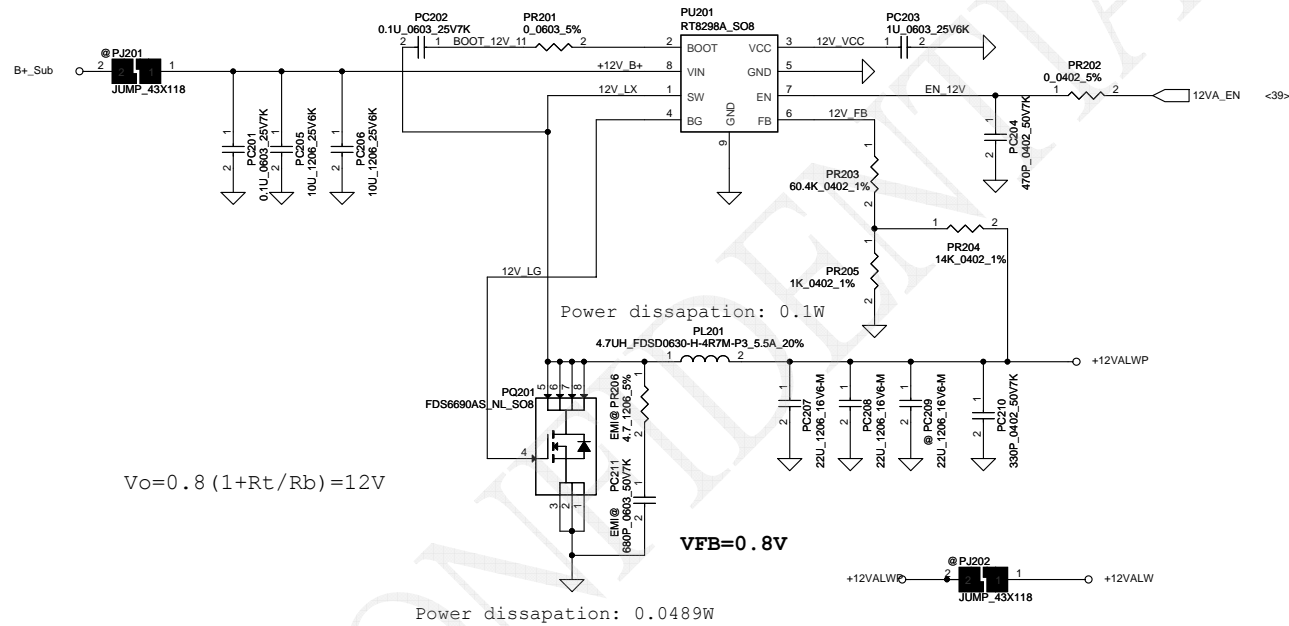
PJP2

CONN@

E-T\_3801K-Q02N-01R

RTC BATT CONNECTER

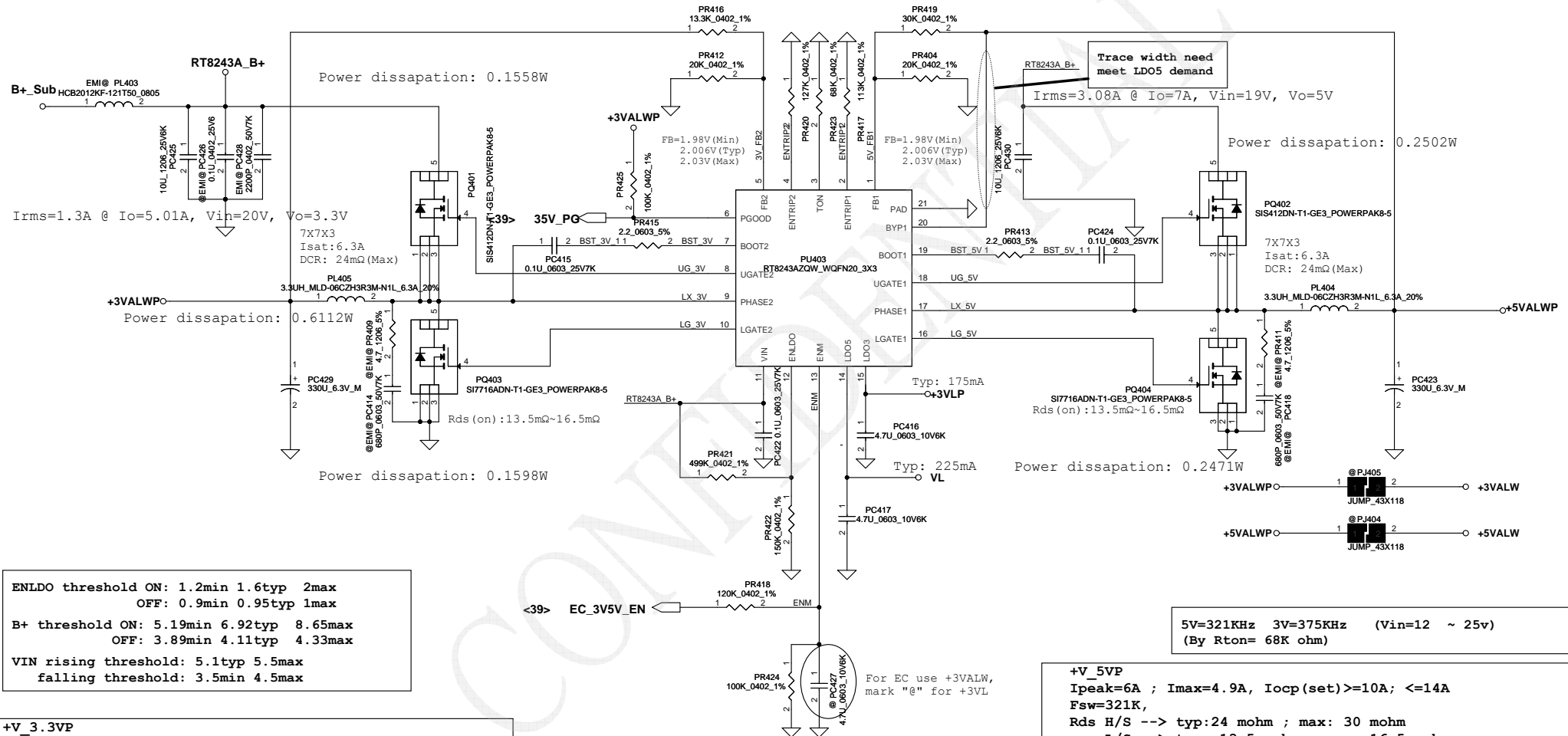
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ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

ENTRIPx adjustment range: 0.5V~3V,  
floating or over 4.5V will shutdown channel.



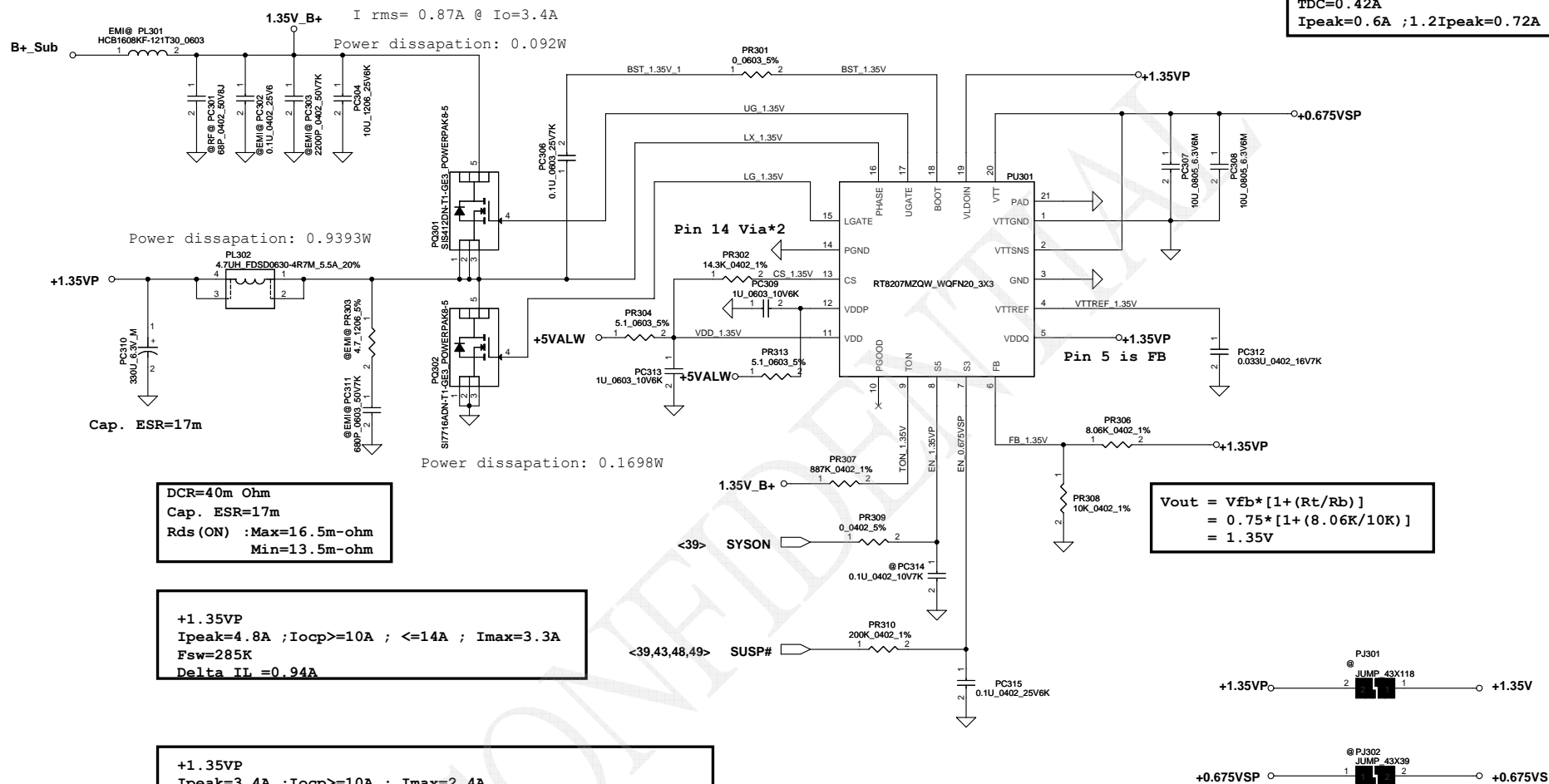
ENLDO threshold ON: 1.2min 1.6typ 2max  
OFF: 0.9min 0.95typ 1max  
B+ threshold ON: 5.19min 6.92typ 8.65max  
OFF: 3.89min 4.11typ 4.33max  
VIN rising threshold: 5.1typ 5.5max  
falling threshold: 3.5min 4.5max

+V 3.3VP  
Ipeak=6A; Imax=3.1A; Iocp(set)>=10A; <=14A  
Fsw=300K  
Rds H/S --> typ:24 mohm ; max: 30 mohm  
L/S --> typ: 13.5 mohm ; max: 16.5 mohm  
Delta IL=[(Vin-Vo)/L]\*[(Vin/Vout)\*T]=2.22A  
LIR=Delta IL/Ipeak=0.37  
L=Vout[1-(Vout/Vin)]/LIR\*Iout\*Fsw=3.3uH  
Cout=[L\*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]  
=379.53uF  
CINBULK=Iload\*Vout\*(Vin-Vout)/(Fsw\*Vin^2\*VINPP)=1.1uF

5V=321KHz 3V=375KHz (Vin=12 ~ 25v)  
(By Rton= 68K ohm)

+V 5VP  
Ipeak=6A ; Imax=4.9A, Iocp(set)>=10A; <=14A  
Fsw=321K,  
Rds H/S --> typ:24 mohm ; max: 30 mohm  
L/S --> typ: 13.5 mohm ; max: 16.5 mohm  
Delta IL=[(Vin-Vo)/L]\*[(Vin/Vout)\*T]=3.54A  
LIR=Delta IL/Ipeak=0.59  
L=Vout[1-(Vout/Vin)]/LIR\*Iout\*Fsw=3.3uH  
Cout=[L\*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]  
=197.26uF  
CINBULK=Iload\*Vout\*(Vin-Vout)/(Fsw\*Vin^2\*VINPP)=1.75uF

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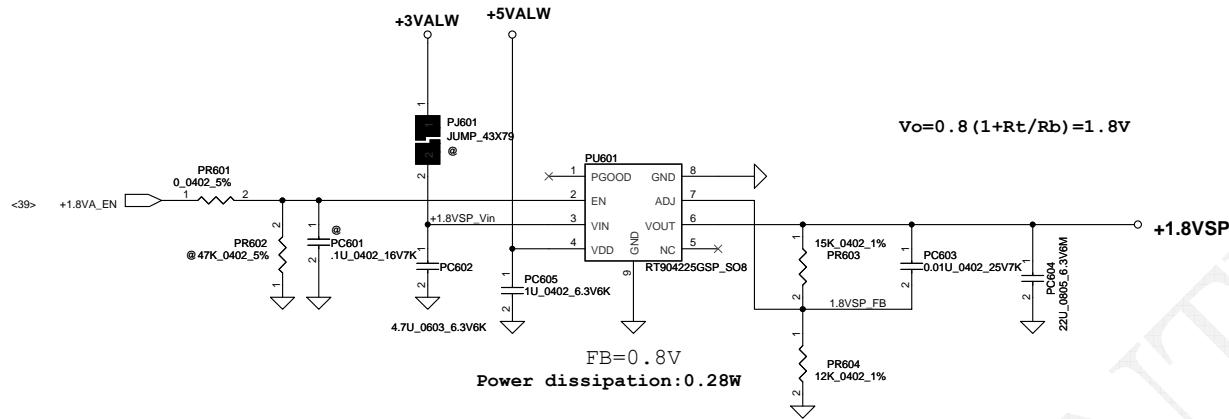


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+1.8VALWP  
Vin = 3.3V  
Iin = 0.075\*1.8/0.9/3.3  
= 0.05A



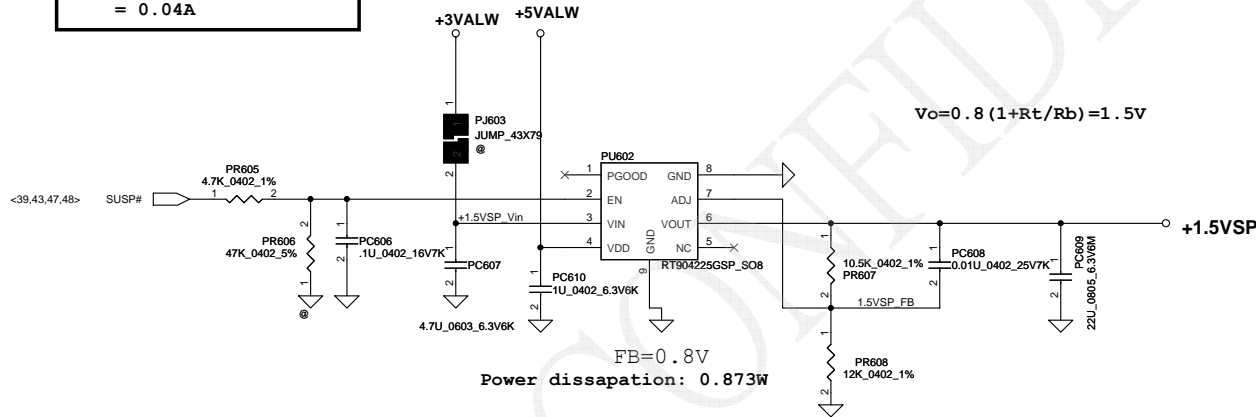
$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t/R_b)] \\ &= 0.8 * [1 + (20K/16K)] \\ &= 1.8V \end{aligned}$$

+1.8VALWP  
Ipeak=0.365A ;  
Iocp>=3.1A

RT9042:  
Quiescent Current (GND Current)  
IQ (typ)=0.6mA, IQ (max)=1.2mA  
PD = (Vin-Vout)\*Iout + Vin\*IQ =0.551W  
θ JA= 75°C/W\*0.551=41.35°C



+1.5VSP  
Vin = 3.3V  
Iin = 0.072\*1.5/0.9/3.3  
= 0.04A



$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t/R_b)] \\ &= 0.8 * [1 + (14K/16K)] \\ &= 1.5V \end{aligned}$$

+1.5VSP  
Ipeak=0.072A  
Iocp>=3.1A

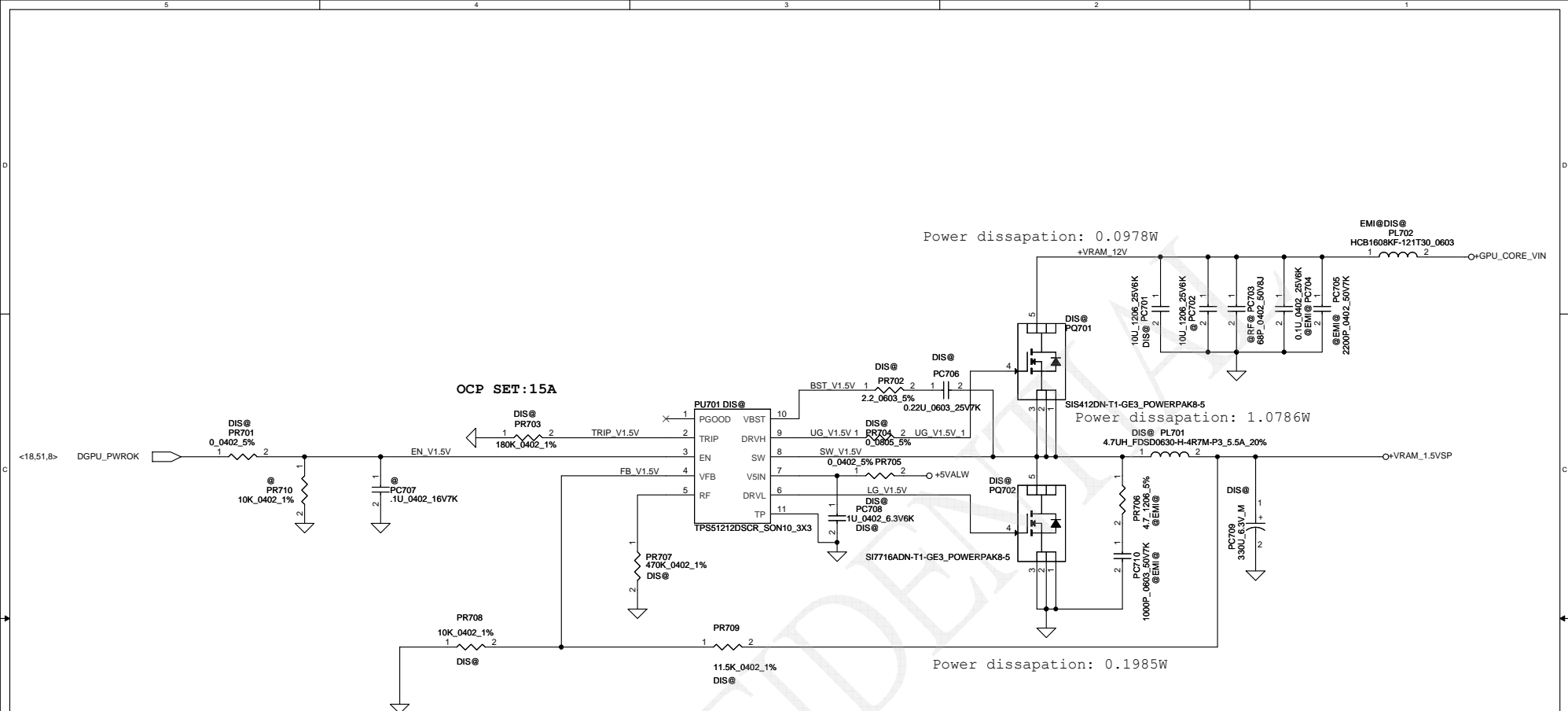
RT9042:  
Quiescent Current (GND Current)  
IQ (typ)=0.6mA, IQ (max)=1.2mA  
PD = (Vin-Vout)\*Iout + Vin\*IQ =0.133W  
θ JA= 75°C/W\*0.551=10.01°C



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Cap. ESR=17m  
 Rds (ON) :Max=15m-ohm  
 Typ=12m-ohm  
 Vtrip range ==> 0.2V ~ 3V  
 <Vo=1.5V> VFB=0.7V  
 $V=0.7 \times (1+11.5K/10K)=1.505V$   
 Fsw=290KHz

Ipeak=4.7A, Imax=3.29A, Iocp=1.2\*Ipeak=5.64A

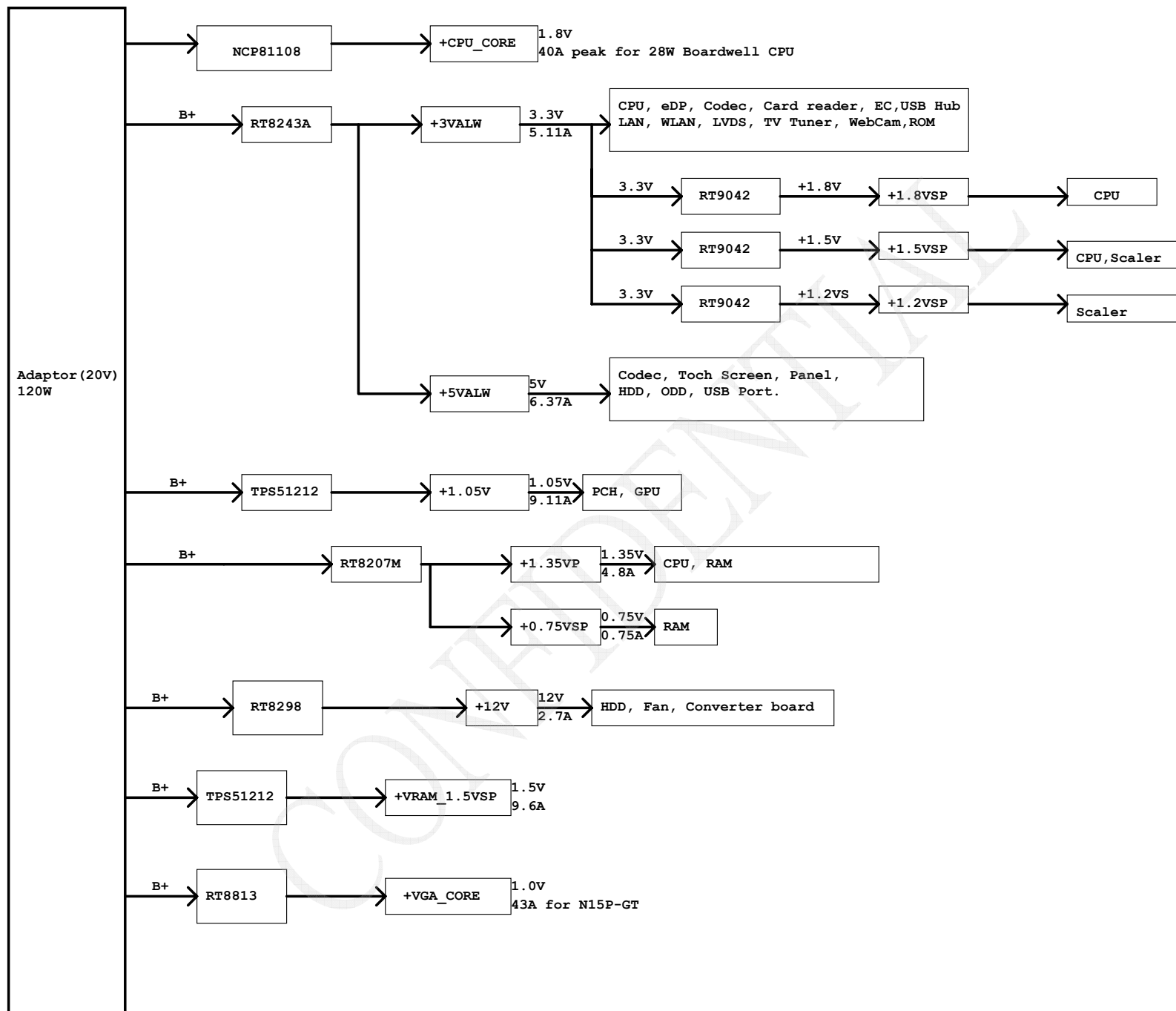
Iocp(set)=5.718A~8.304A

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20131104	50	Change the PU901 to SA00007GK00	for PWR Design change
2.	20131104	51	Change the PC809,PC810 to SGA00004200	for PWR Design change
3.	20131104	46	Change the PR418 to 120K,PR424 to 100K	for PWR Design change
4.	20131104	51	Change the PR918,920 to 64.9K; PC910 to 680P; PR912 to 24.9K	for PWR Design change
5.	20131104	50, 51	Change the PL803 , 804, PL902,PL904 to SH000001K00	for Matirial EOL
5.	20131105	50	Change the PC909 to 0603 1uF	for PWR Design change

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